Problem Solving Tools Applied to Microfabrication

Presented by
Southwest Center for Microsystems Education
-SCME-
March 2013

SCME is a National Science Foundation Advanced Technological Education (ATE) Program at the University of New Mexico.

We offer professional development and educational materials to excite and engage high school, community college and university students in the field of Microsystems (MEMS) technology.

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Our Presenters

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Instructional Designer, SCME and retired Chair for the Manufacturing Technology Program – Central New Mexico Community College

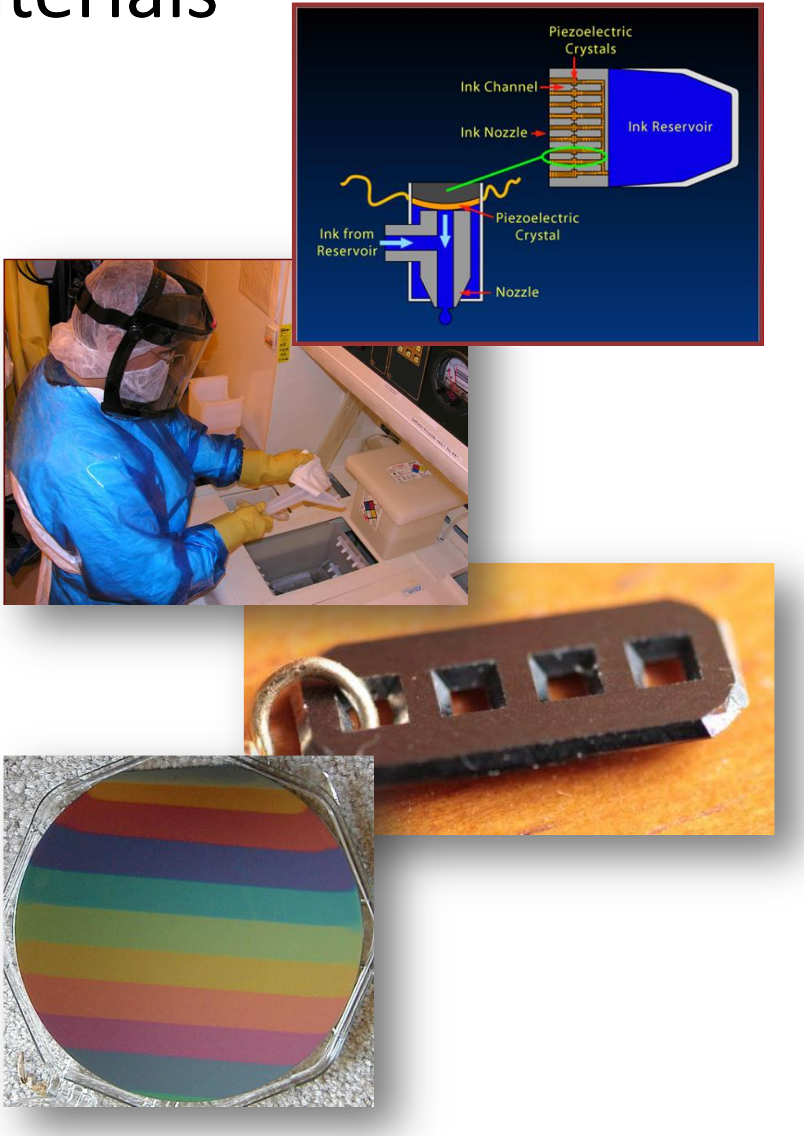
What will we cover today?

- What SCME can do for you
- How to use the problem-solving process and various tools to solve an out-of-control situation in the fabrication of a MEMS pressure sensor.

SCME
Southwest Center for
Microsystems Education

Educational Materials

- SCME Learning Modules
  - Informational Units / lessons
  - Supporting activities
  - Supporting assessments
- ~40 Modules in the areas of
  - Safety
  - Microsystems Introduction
  - Microsystems Applications
  - Bio MEMS
  - Microsystems Fabrication
- 11 Instructional Kits
- All are available @ scme-nm.org

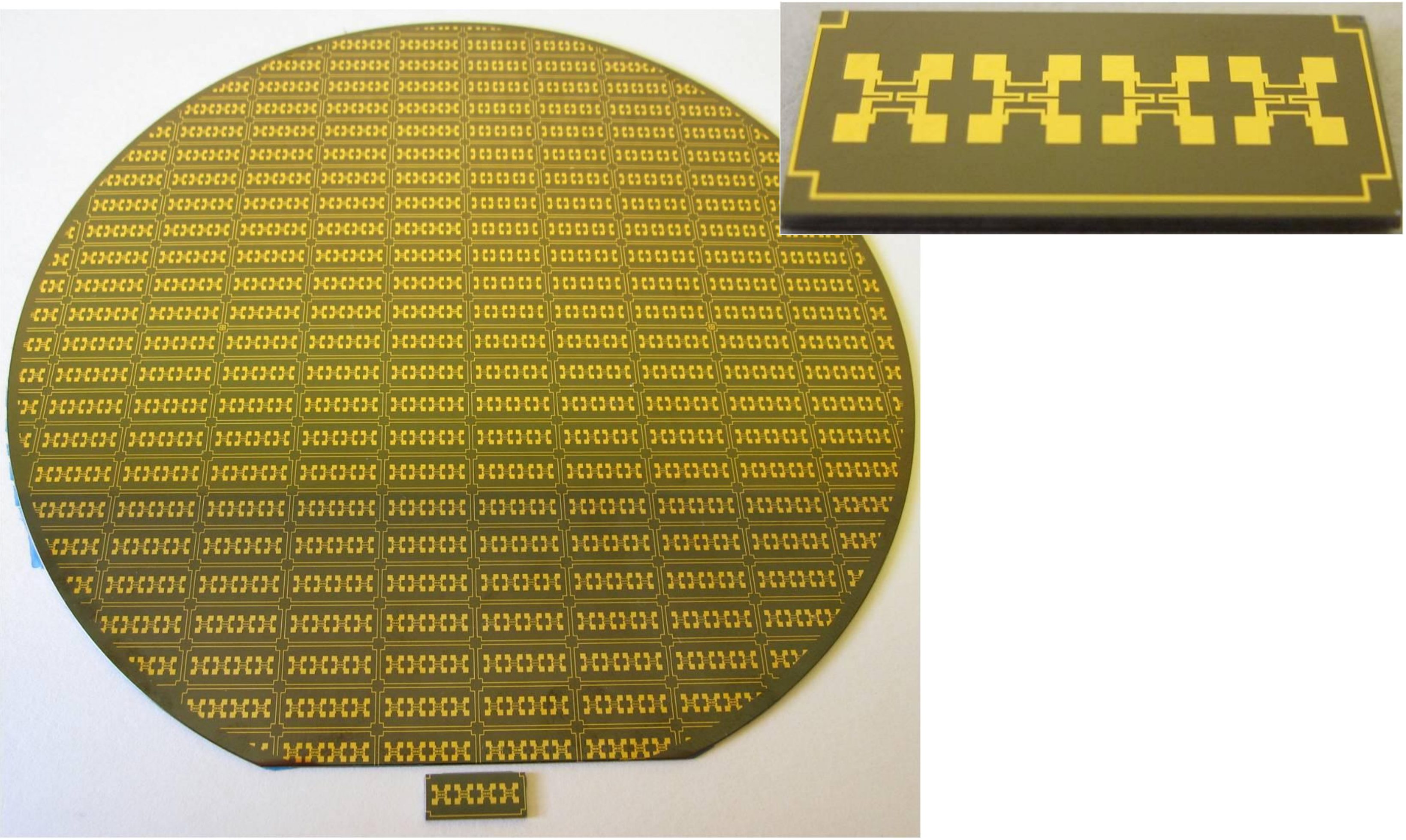


Southwest Center for
Microsystems Education

Professional Development

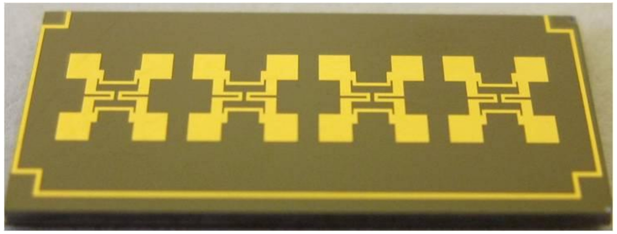
- 4 to 5-day workshops
- 2-day workshops
- 1-day workshop
- Conferences and conference workshops
- Create hubs at other colleges to teach our workshops
- Webinars
- SCME on YouTube (https://www.youtube.com/user/scme2012)

Final Pressure Sensor Wafer



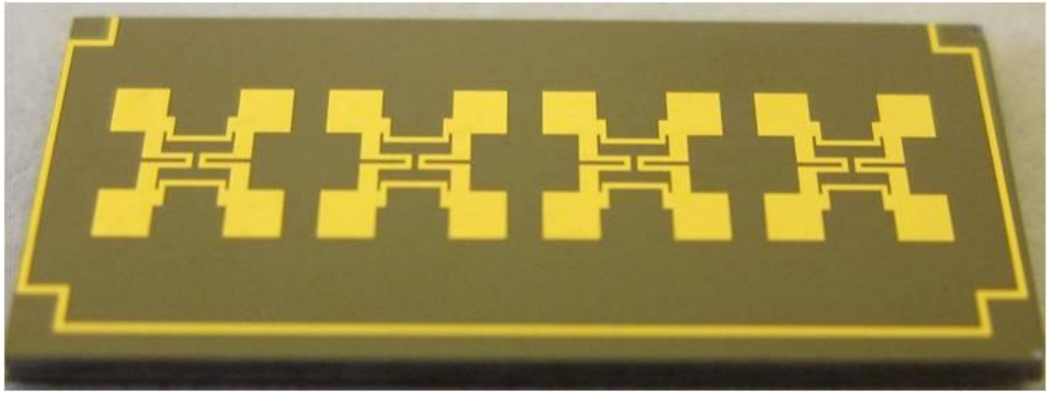
Final Test Process

- Wafers are tested in batches (6 lots of 24 wafers missed any wafers previously scrapped)
- *Approximately* 150 die / wafer
- 4 pressure sensors / die
- 1 defective pressure sensor yields defective die
- Data collected and recorded
  - Number of die tested / wafer
  - Number of die rejected / wafer
  - The type of “defect” that caused the rejection



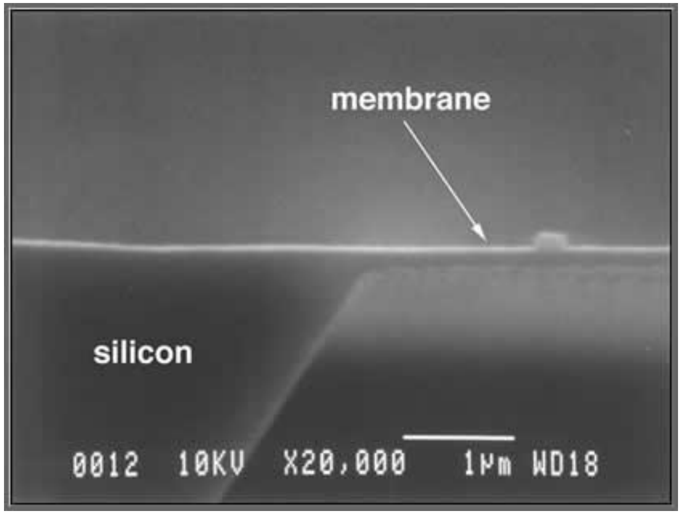
Defect vs. Defective

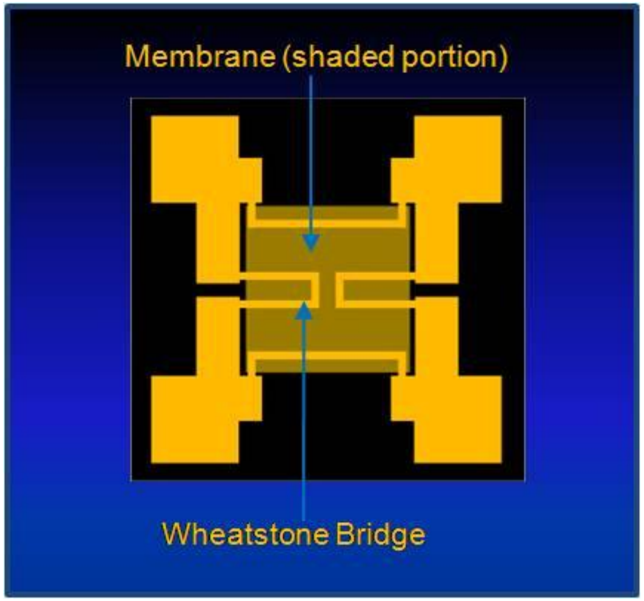
- A defect is any nonconformance of the unit of product with the specified requirements.
- A defective is a unit of product which contains one or more defects.



Pressure Sensor

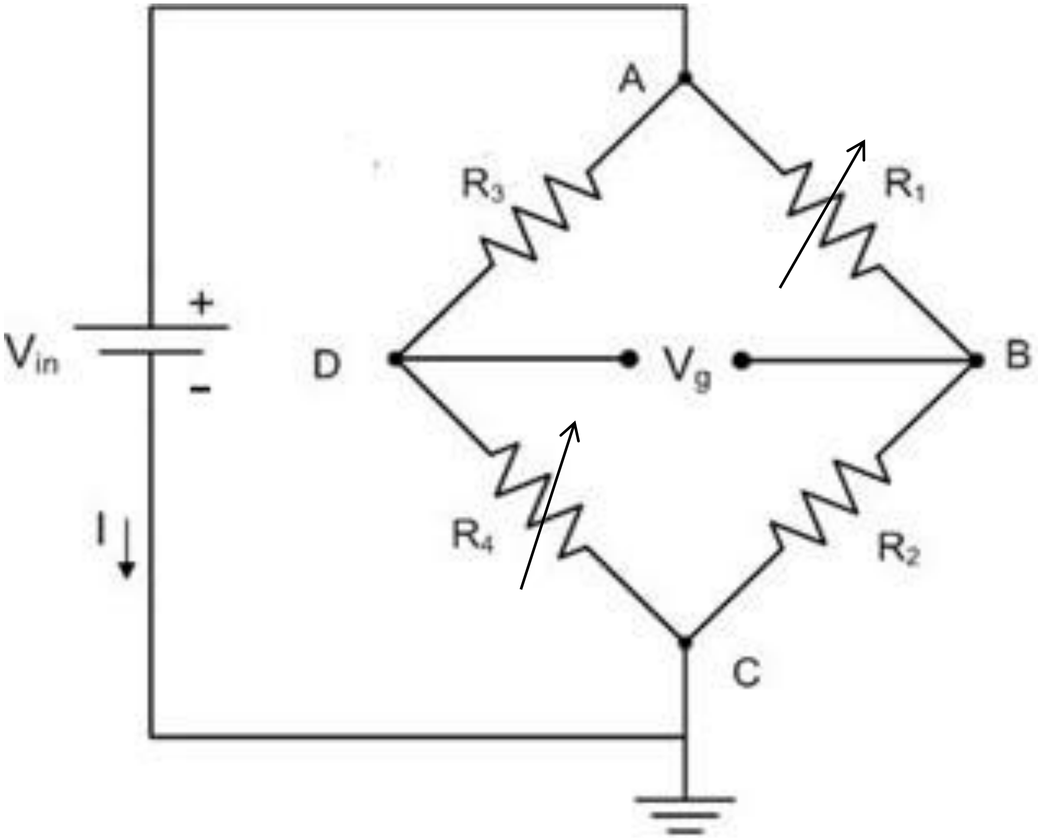
- Wheatstone bridge electronic sensing circuit
  - Conducting metal
    - 4000 Angstroms of gold on top of
    - 100 Angstroms of Chrome
  - 4 Pads for leads
  - 4 Resistors (2 fixed, 2 variable)
- Membrane
  - Silicon Nitride
- Reference chamber
  - Etch away a hole to act as the chamber

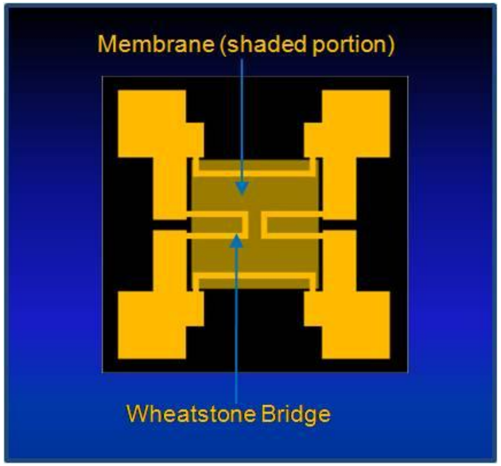




Wheatstone Bridge Sensing Circuit

- Input voltage (Vin)
- Output voltage (Vg)
- Variable resistors (R1 and R4)
- Fixed resistors (R2 and R3)





Testing a Pressure Sensor

- V_{in} = 5 volts
- V_g range = 0 to 50 mV

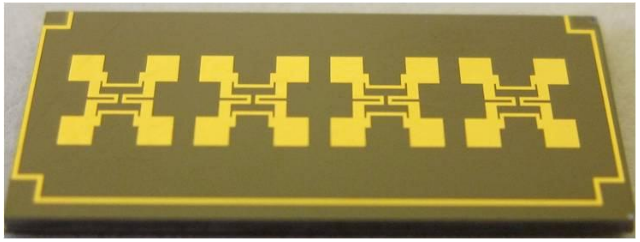
List of Defects

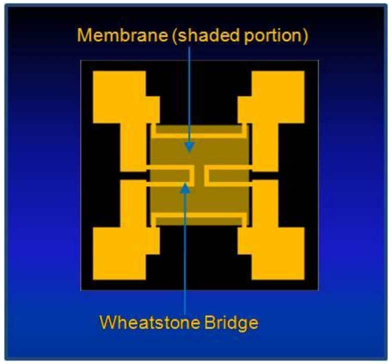
$\Delta V_g < 20$ mV

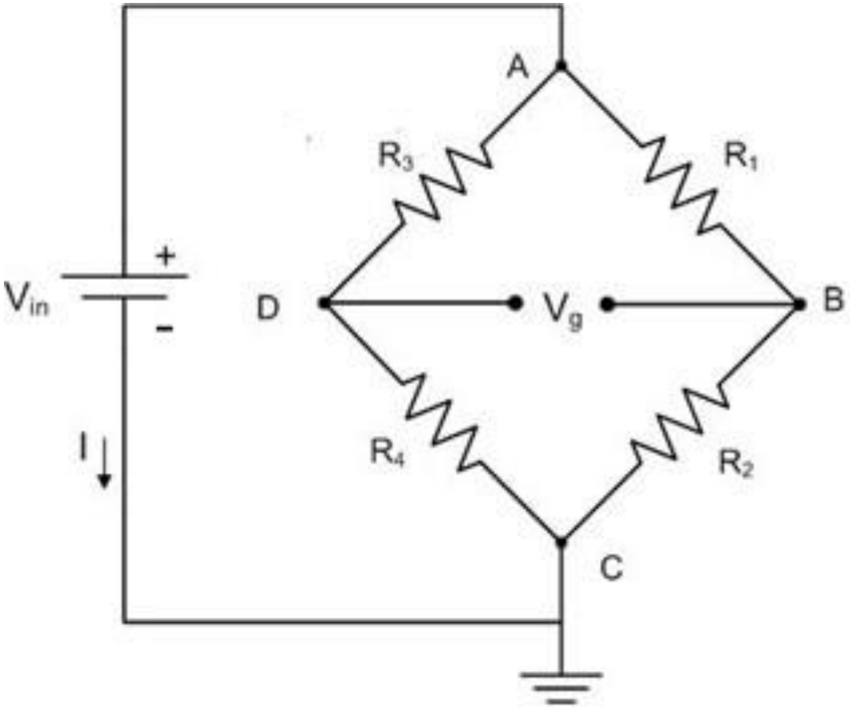
$\Delta V_g = 0$ V

$V_g = 50$ mV regardless of the applied pressure

$V_g = 5$ V







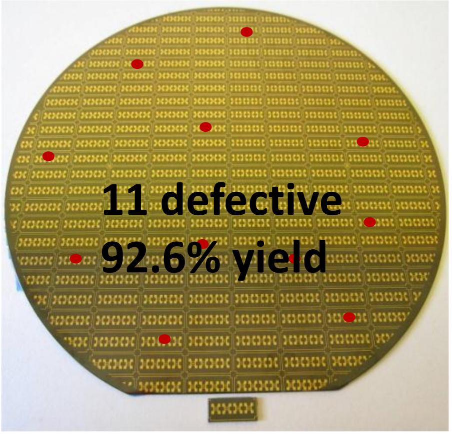
Calculating Die Yield

- Yield per wafer = # good die/total # die
- Yield per batch = mean of wafer yields
- Range per batch = highest yield wafer – lowest yield wafer
- Given a batch of 139 wafers.
- Each die on each wafer was tested and the yield per wafer was calculated.
  - Wafer 79 had 148 die and 14 die were rejected
  - Wafer yield = (148 – 14)/148 = 0.9054 or 90.5% yield
- Total Die Yield (µ) = The sum of the wafer yields (Xn) / total number of wafers tested (n = 139)

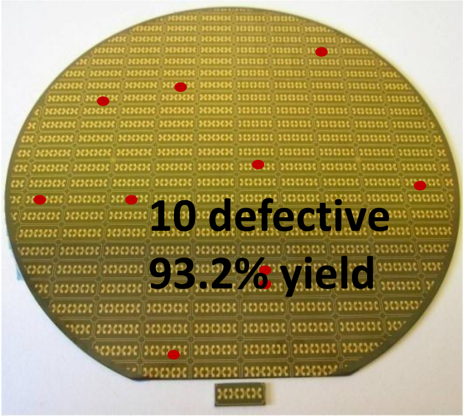
$$\mu = \frac{\Sigma x_n}{n}$$

Final Test Wafers

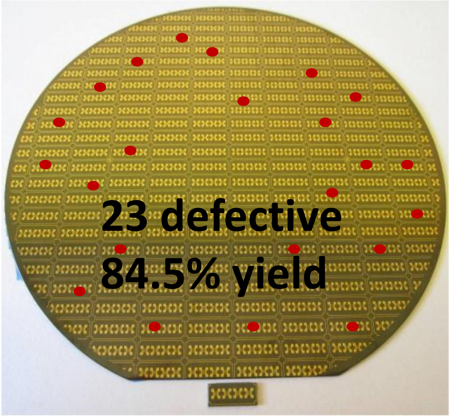
24 defective
83.8% yield



11 defective
92.6% yield



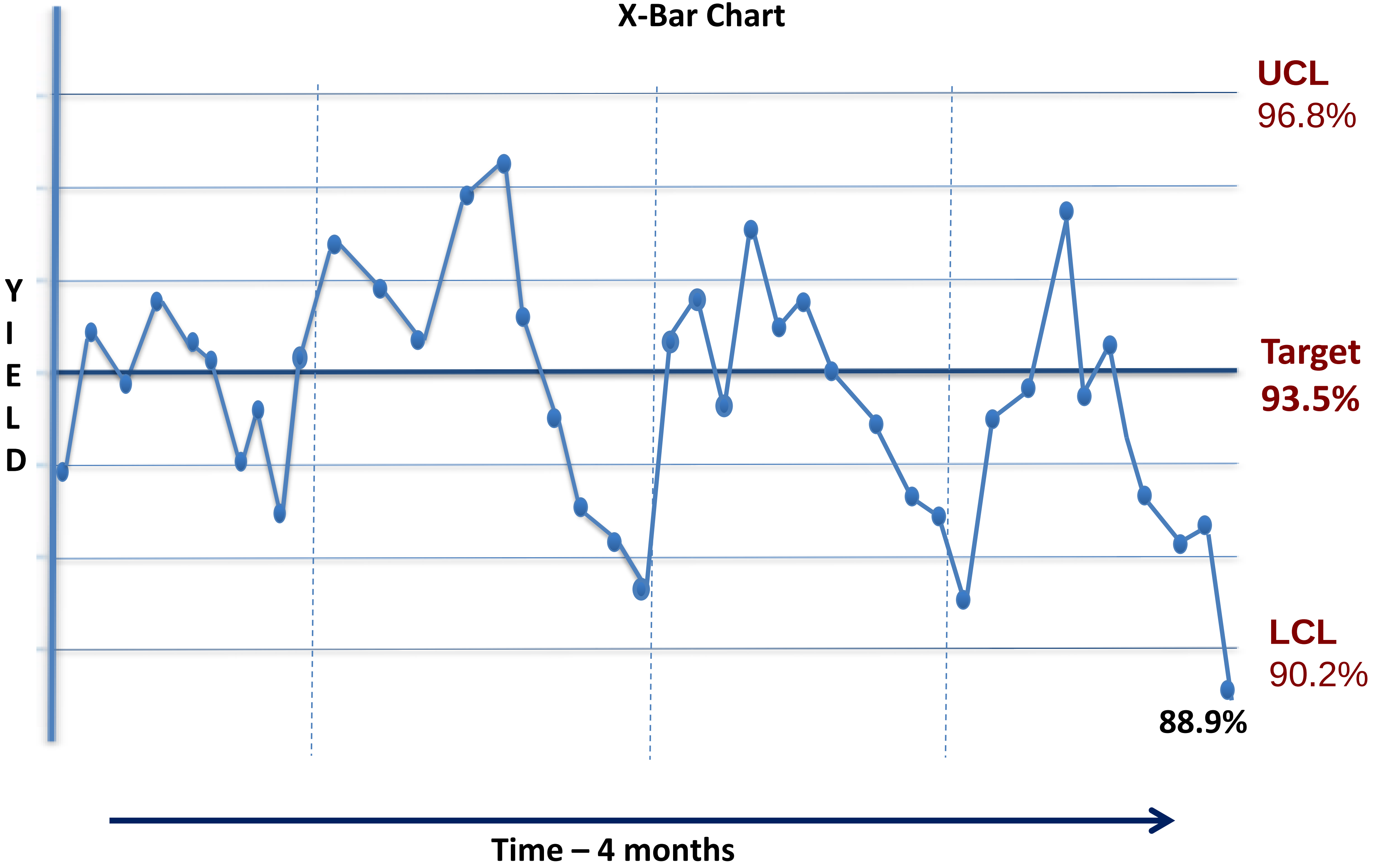
10 defective
93.2% yield



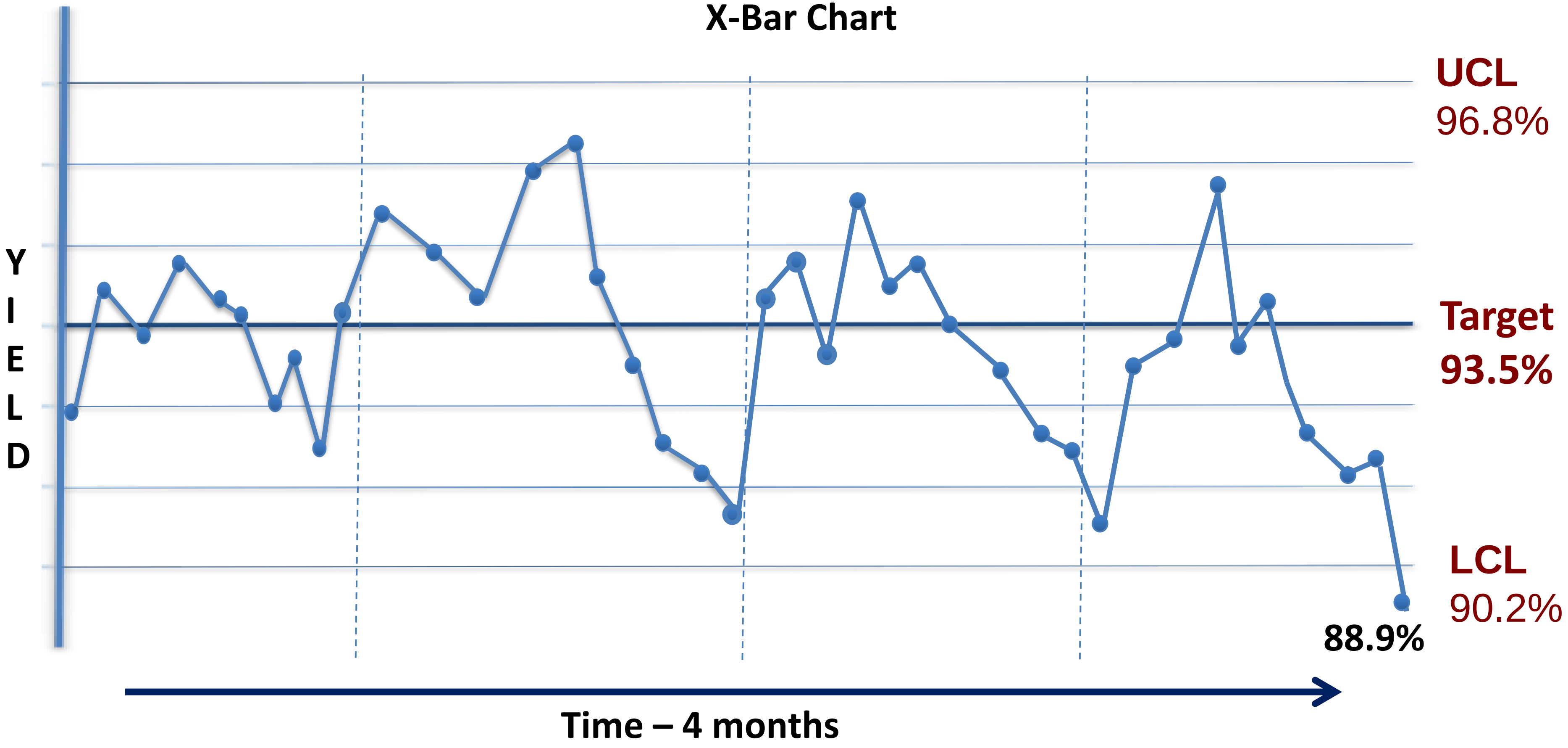
23 defective
84.5% yield

150 die/wafer: 88.9% is an average of ~133 good die/wafer or an average of 17 defective die per wafer.

Batch DIE Yield – MEMS Pressure Sensors
X-Bar Chart



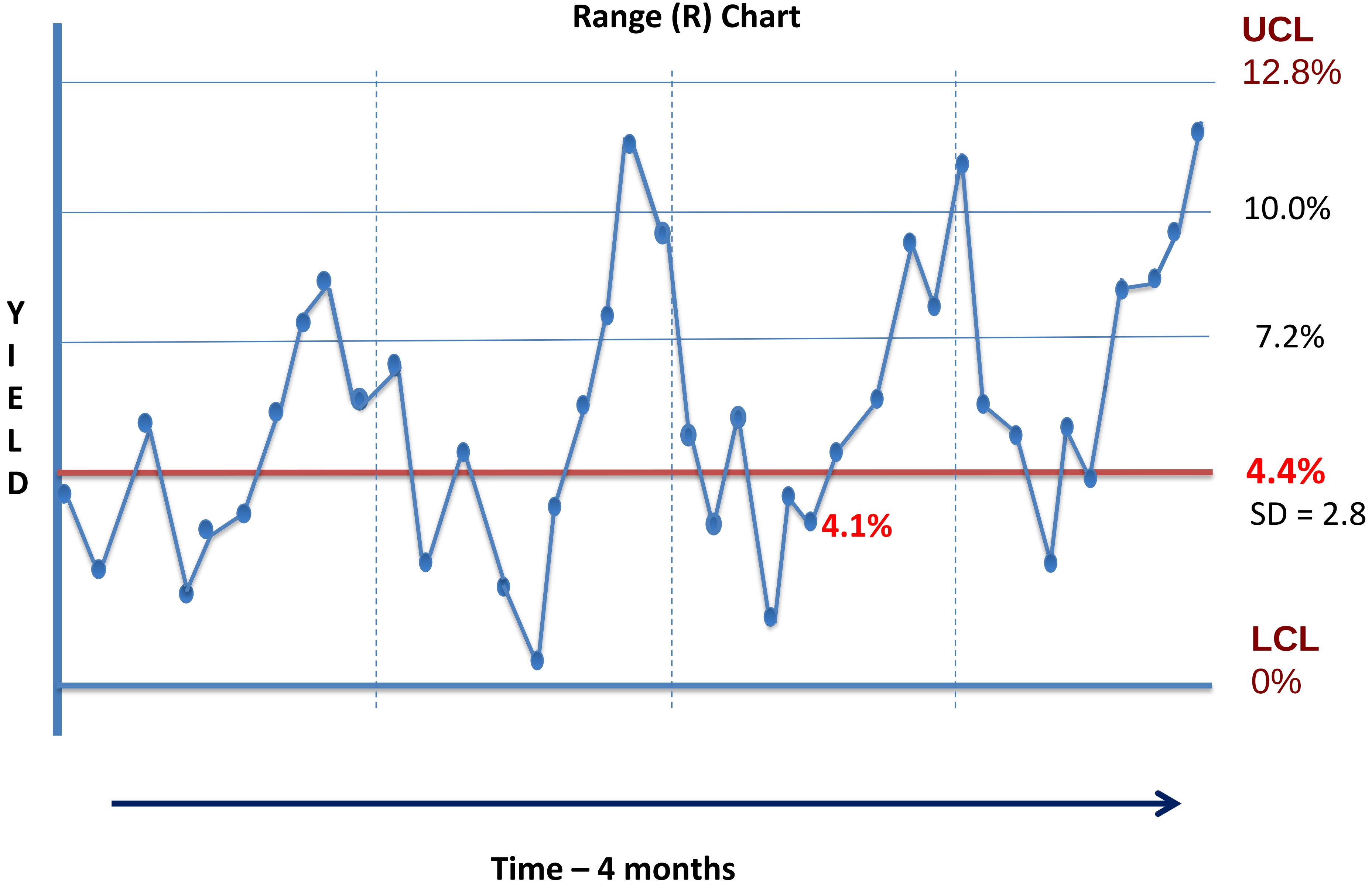
Batch DIE Yield – MEMS Pressure Sensors
X-Bar Chart



Assuming the yield to be a normal distribution, what percent of our batch yields over time, should fall between the upper and lower control limits?

a. 68.6%
b. 95.0%
c. 98.9%
d. 99.7%

Batch DIE Yield – MEMS Pressure Sensors
Range (R) Chart



Shewhart Rules

aka Western Electric Rules (WECO)

8 Rules to Signal an Out of Control Process

Rule 1: A single point outside the *μ±3σ* zone.

Rule 2: Two out of three successive points outside *μ±2σ* zone.

Rule 3: Four out of five successive points outside *μ±1σ* zone.

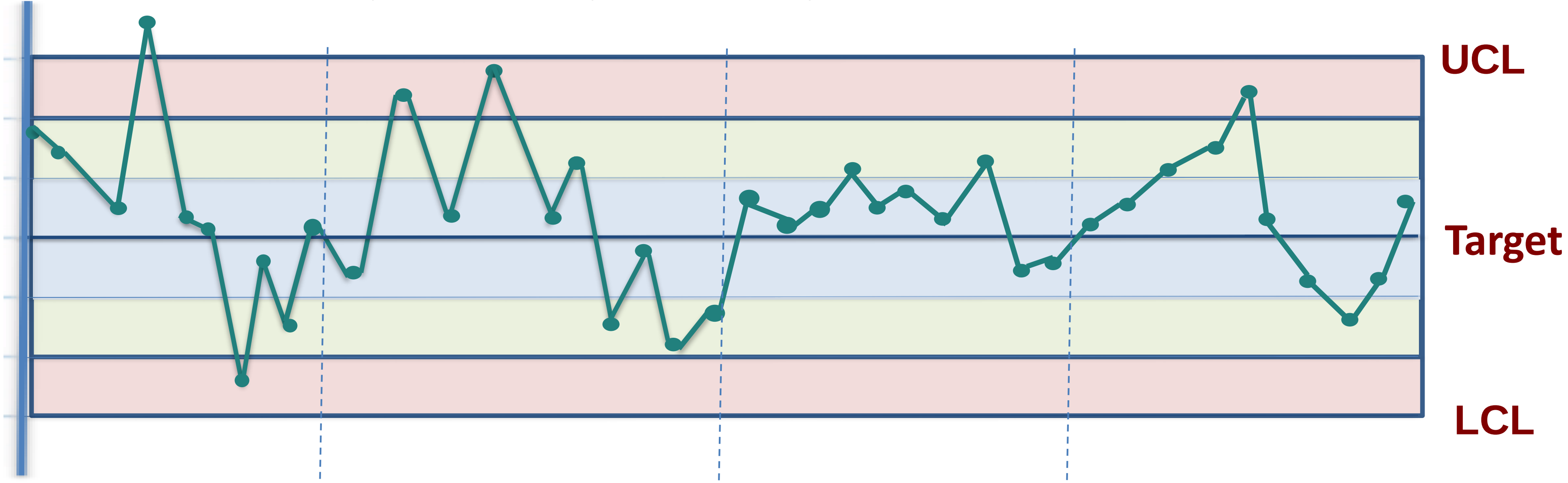
Rule 4: Eight or more successive numbers either strictly above or strictly below the mean (the center).

Rule 5: Six or more successive numbers showing a continuous increase or continuous decrease.

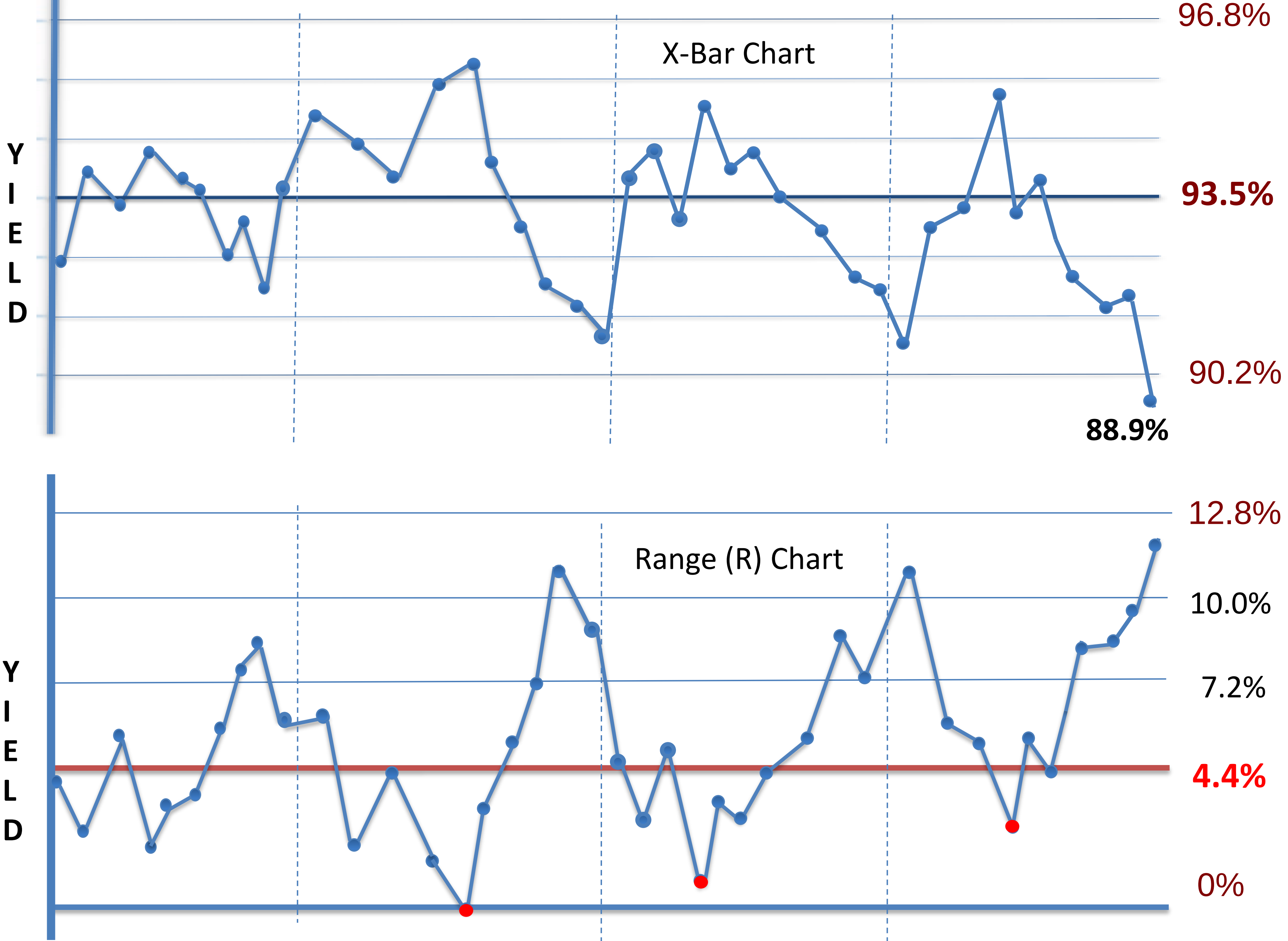
Rule 6: Fourteen or more successive numbers that oscillate in size (i.e. smaller, larger, smaller, larger)

Rule 7: Eight or more successive numbers that avoid *μ±1σ* zone.

Rule 8: Fifteen successive points fall into *μ±1σ* zone only, to either side of the centerline.



Batch DIE Yield – MEMS Pressure Sensors



Six Steps to Problem Solving

Recognize the a Problem Exists

Analyze the Problem

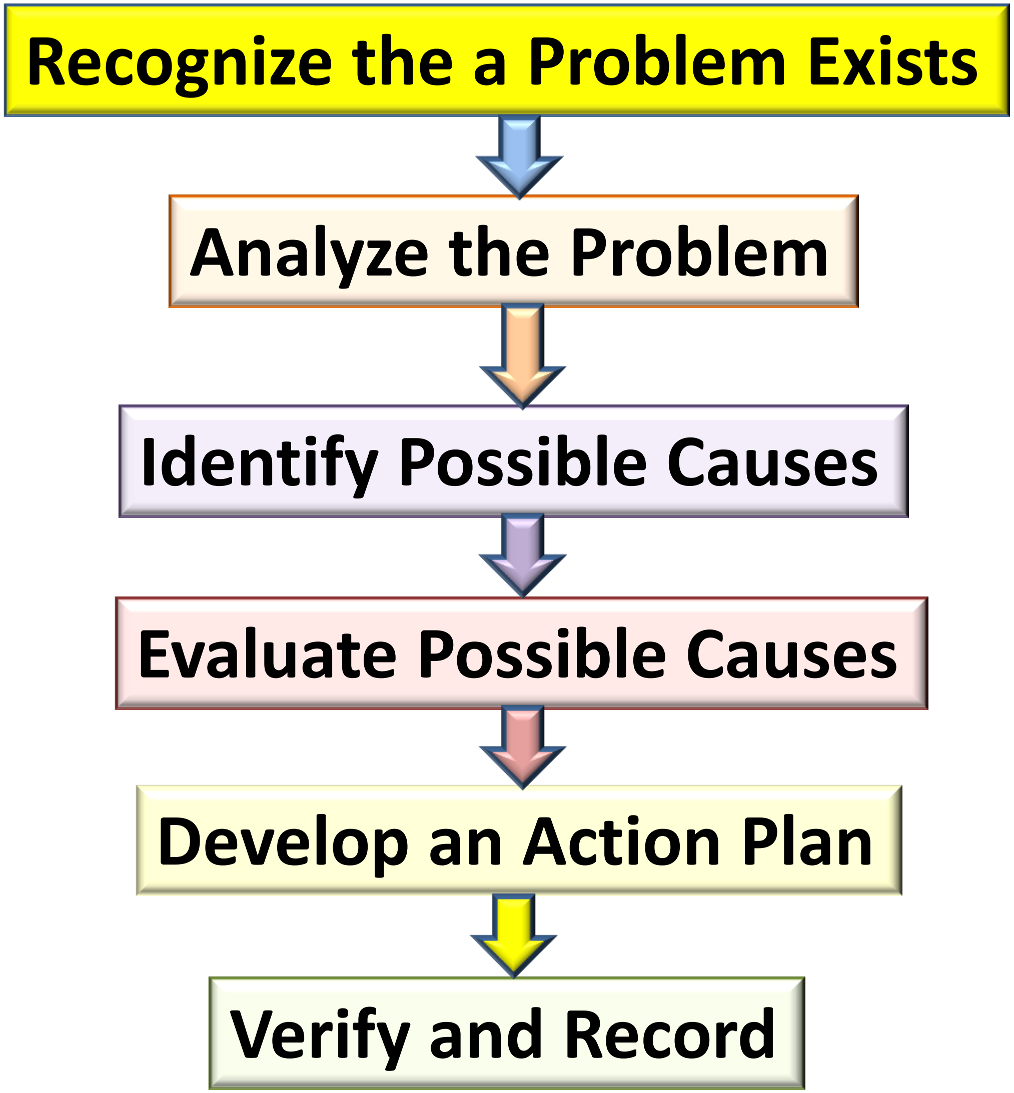
Identify Possible Causes

Evaluate Possible Causes

Develop an Action Plan

Verify and Record

1. Recognize the Problem Exists



Recognize the a Problem Exists

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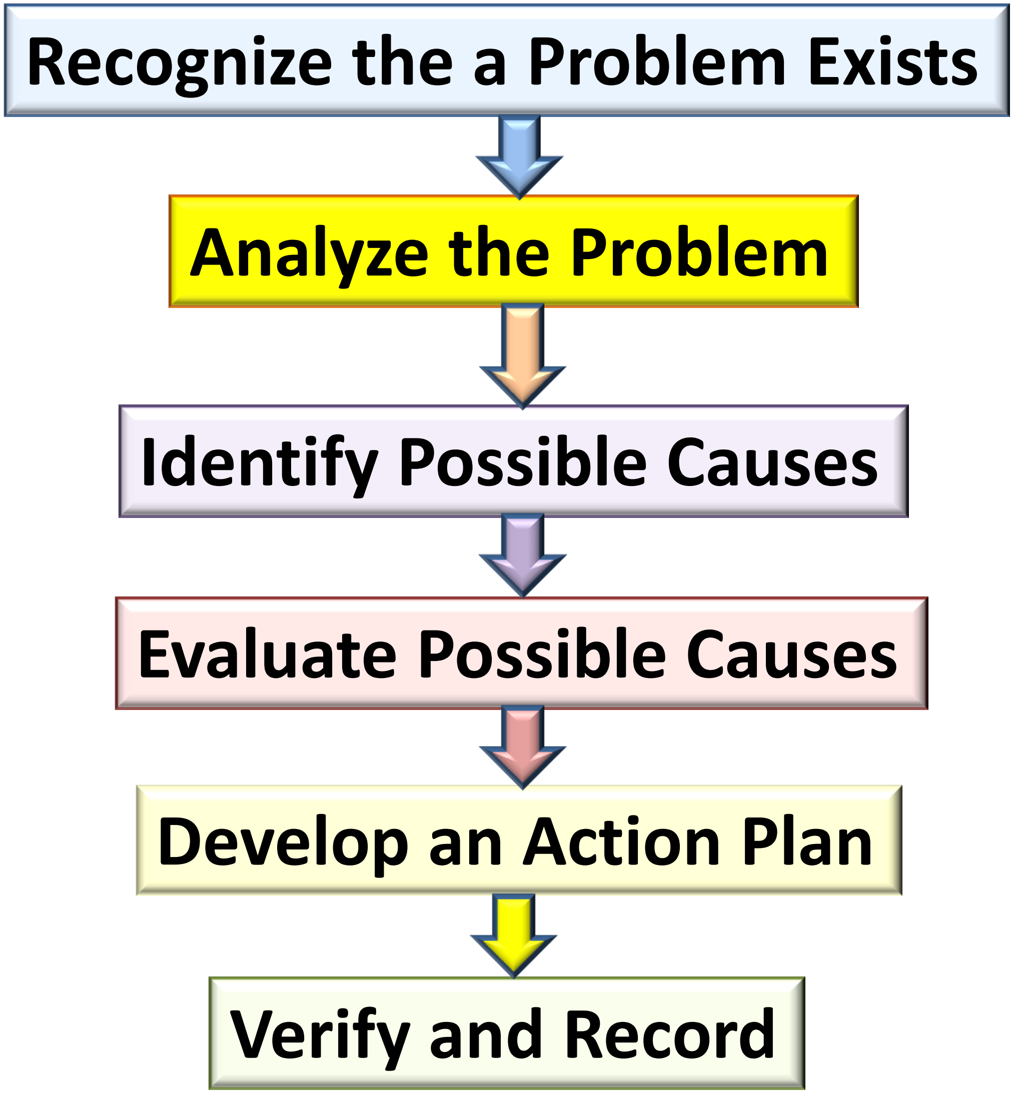
Problem Statement

The die yield in the final inspect has dropped below the statistically acceptable Lower Control Limit (LCL) of 90.3% to a yield of 88.9%.

- Our OOC point is also the 4th consecutive data point below -1 standard deviation.
- On the R-chart, the range of the last batch is the 4th consecutive point above 1 standard deviation.
- The die yield in the final inspect has been fluctuating, but in control, over the past 3 months, with short potential trends and oscillations.

2. Analyze the Problem



Recognize the a Problem Exists

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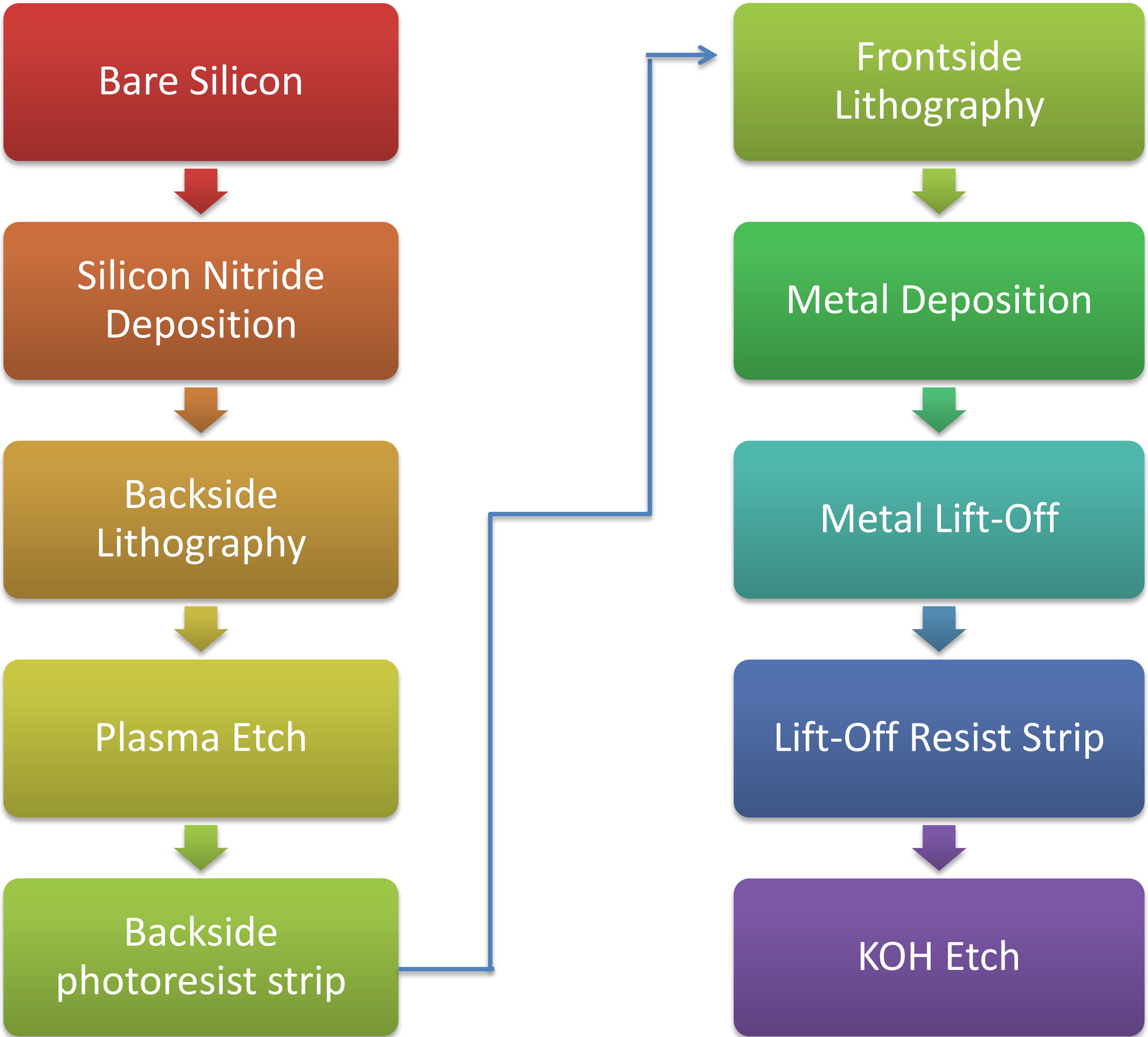
Review of the PS Process



Bare Silicon

Silicon Nitride Deposition

Backside Lithography

Plasma Etch

Backside photoresist strip

Frontside Lithography

Metal Deposition

Metal Lift-Off

Lift-Off Resist Strip

KOH Etch

Review of the PS Process

Bare Silicon

- Standard monocrystalline silicon wafer (100) crystal orientation
- Crystal orientation is important for bulk etch at the end of process
- No Data Tracked

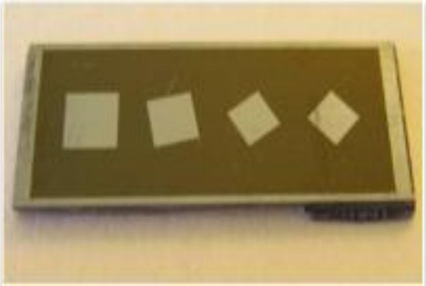
Silicon Nitride Deposition

- $1\mu m$ SiN deposited on both sides of wafer
- Front SiN will act as pressure sensor membrane
- Back SiN will act as the hard pattern mask protecting the areas of the wafer not being etched during the anisotropic etch
- Data Tracked: SiN thickness & uniformity, gas flow rate, temperature

Images courtesy of UNM-MTTC Laboratory

Review of the PS Process

Backside Photolithography



- Produces the hole *patterns* for the Pressure Sensor Cavity
- Data Tracked: Resist thickness & uniformity, exposure time
- Visual Inspection Data: Alignment pass or fail, critical dimension, defects (particles, holes, underdeveloped or overexposed)

Plasma Etch

Etches backside SiN layer through the holes exposing the silicon wafer.

Data Tracked: Pressure, RF level

Visual Inspection Data: Pass/Fail

Backside Photoresist Strip

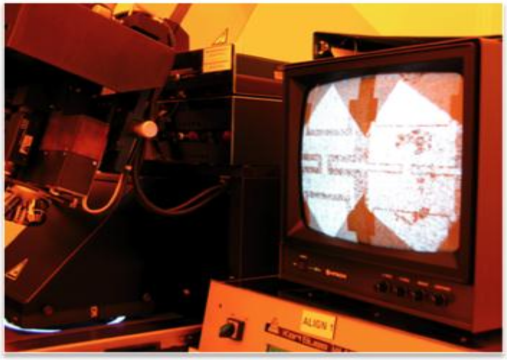
Aggressively removes the remaining photoresist.

Visual Inspection Data: Pass/Fail

Images courtesy of UNM-MTTC Laboratory

Review of the PS Process

Frontside Photolithography



- Produces the Wheatstone bridge *patterns* for the Circuit
- Data Tracked: Resist thickness & uniformity, exposure time
- Visual Inspection Data: Alignment pass or fail, critical dimension, defects (particles, holes, underdeveloped or overexposed)

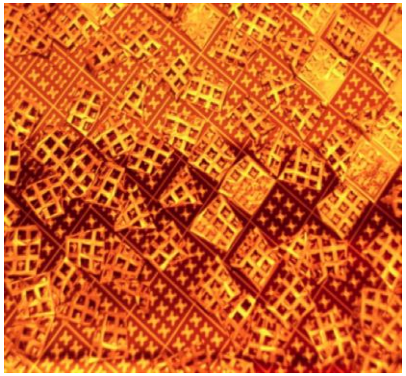
Metal Deposition

Deposit 100 angstroms of chrome followed by 4000 angstroms of gold to be used as the Wheatstone bridge circuit.

Data Tracked: pressure, Thickness & uniformity

Visual Inspection Data: Particles

Metal Lift-Off



The excess metal not used as the circuit is removed

Data Tracked:

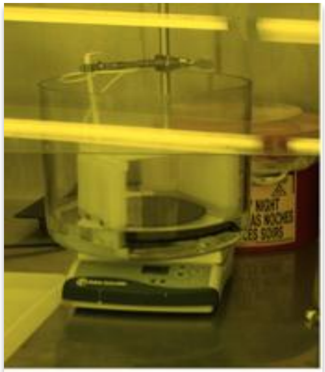
Particle count temperature

Visual Inspection Data: contamination, defects

Images courtesy of UNM-MTTC Laboratory

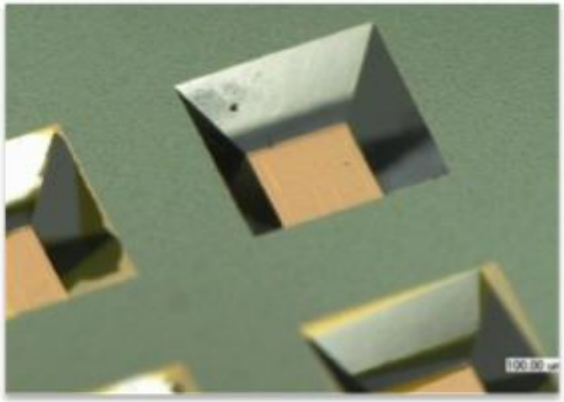
Review of the PS Process

Lift-Off Resist Strip



- The remaining LOR is removed using a developer solution
- Visual Inspection Data: Pass/Fail

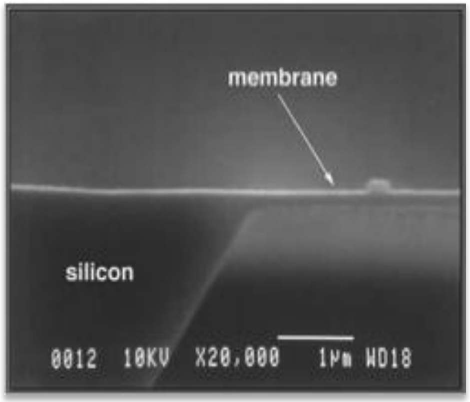
KOH Etch



- Wafers are submerged in a **heated** (KOH) bath
- 105°C - 2Hrs
- 95°C- 1.5Hrs
- 80°C- 45Min
- Data Tracked: SPC of process Temperatures
- Visual Inspection: Final Inspect

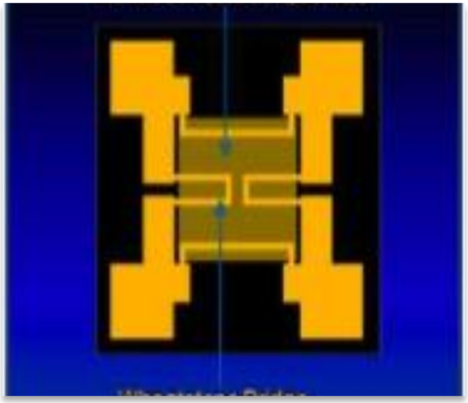
Images courtesy of UNM-MTTC Laboratory

Pressure Sensor Features



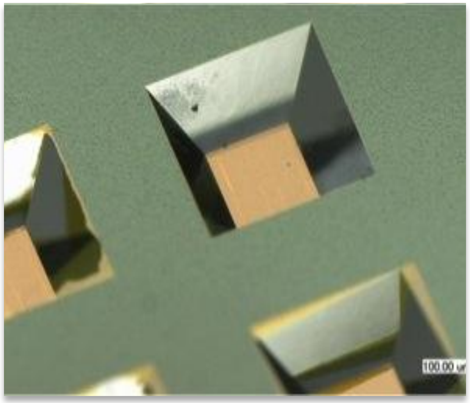
Pressure Sensor

Membrane



Wheatstone Bridge

Circuit

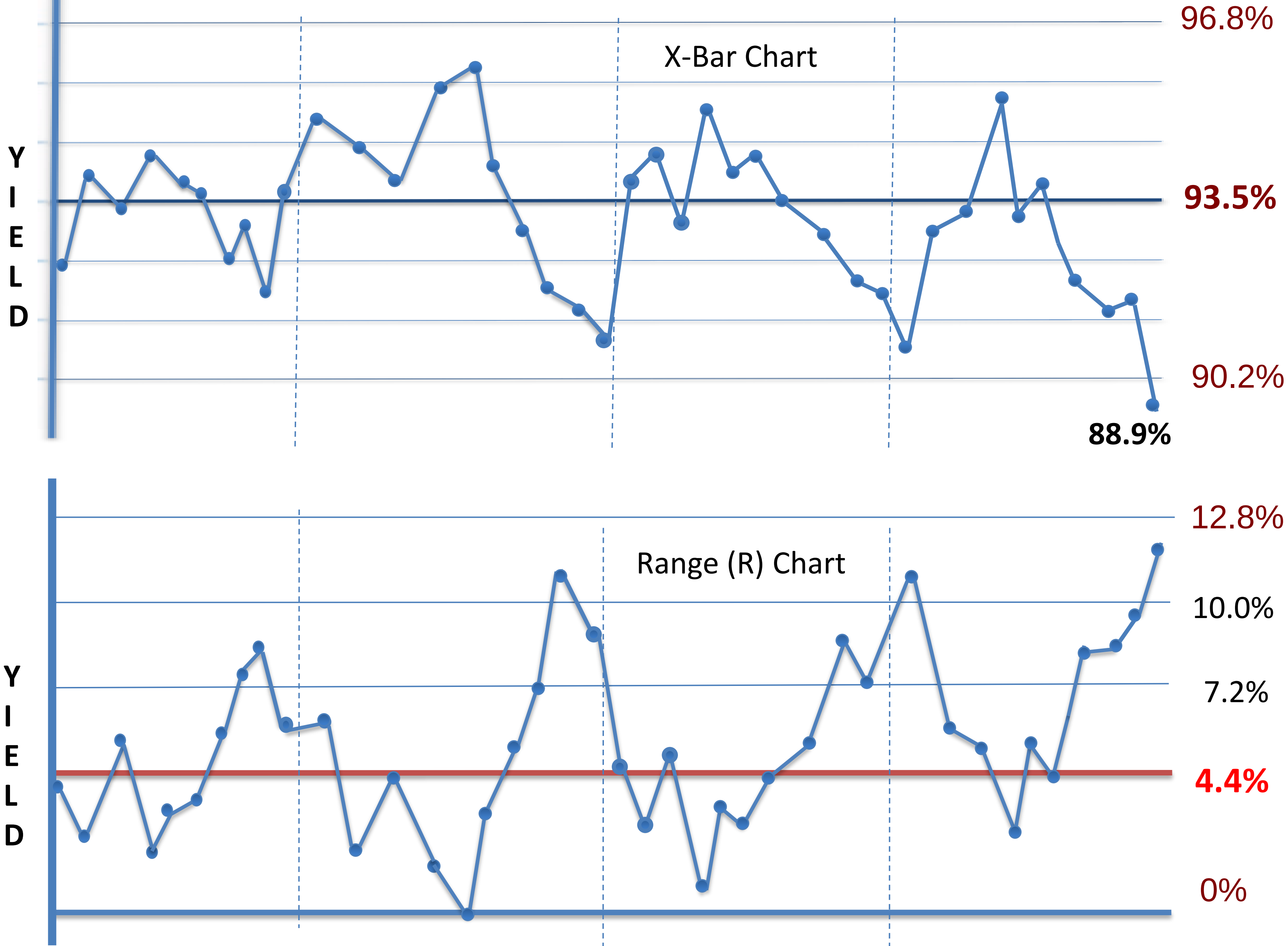


Pressure Sensor

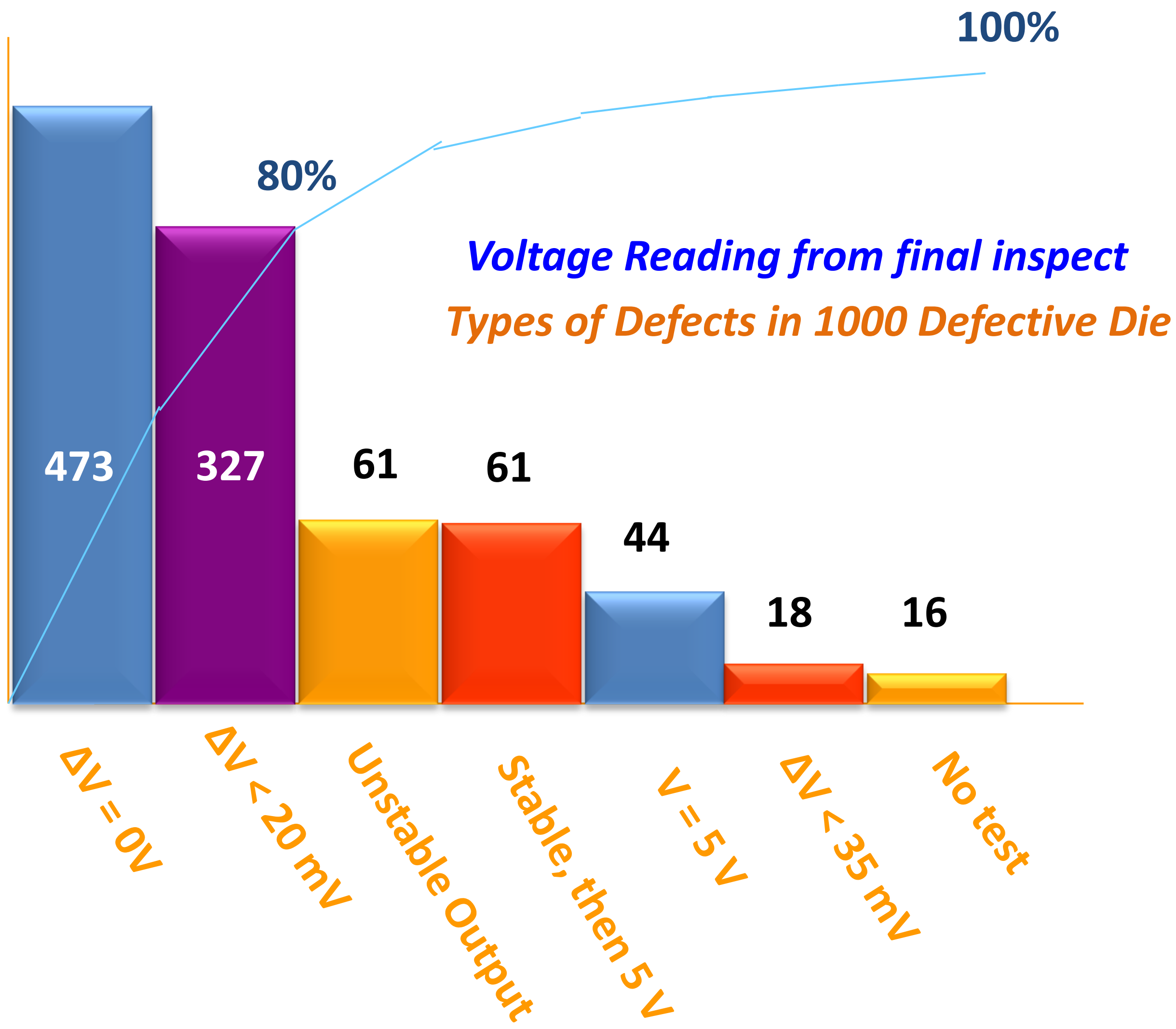
Cavity

Images courtesy of UNM-MTTC Laboratory

Batch DIE Yield – MEMS Pressure Sensors



Pareto Chart of Defects



3. Identify Possible Causes

Recognize the a Problem Exists

Analyze the Problem

Identify Possible Causes

Evaluate Possible Causes

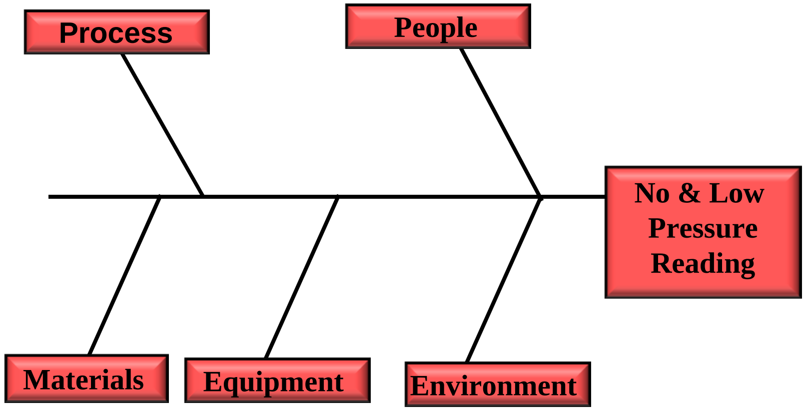
Develop an Action Plan

Verify and Record

Brainstorm No & Low Voltage Reading

No CHANGE in output voltage

Low CHANGE voltage



4. Evaluate Possible Causes

Recognize the a Problem Exists

Analyze the Problem

Identify Possible Causes

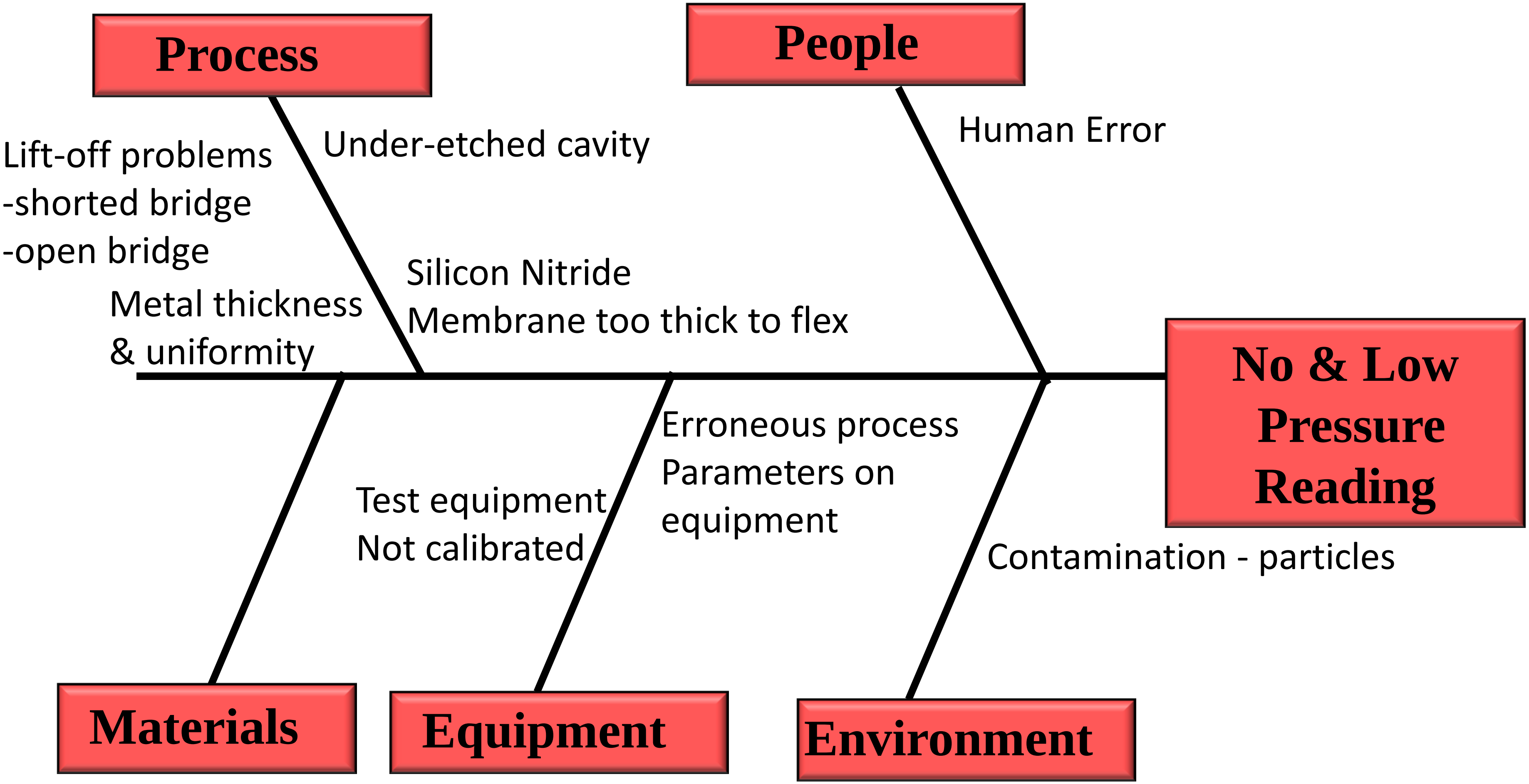
Evaluate Possible Causes

Develop an Action Plan

Verify and Record

Cause and Effect

Factors Affecting No Pressure Reading



Process

Under-etched cavity

Lift-off problems
-shorted bridge
-open bridge

Metal thickness
& uniformity

Silicon Nitride
Membrane too thick to flex

People

Human Error

No & Low Pressure Reading

Materials

Equipment

Test equipment
Not calibrated

Erroneous process
Parameters on
equipment

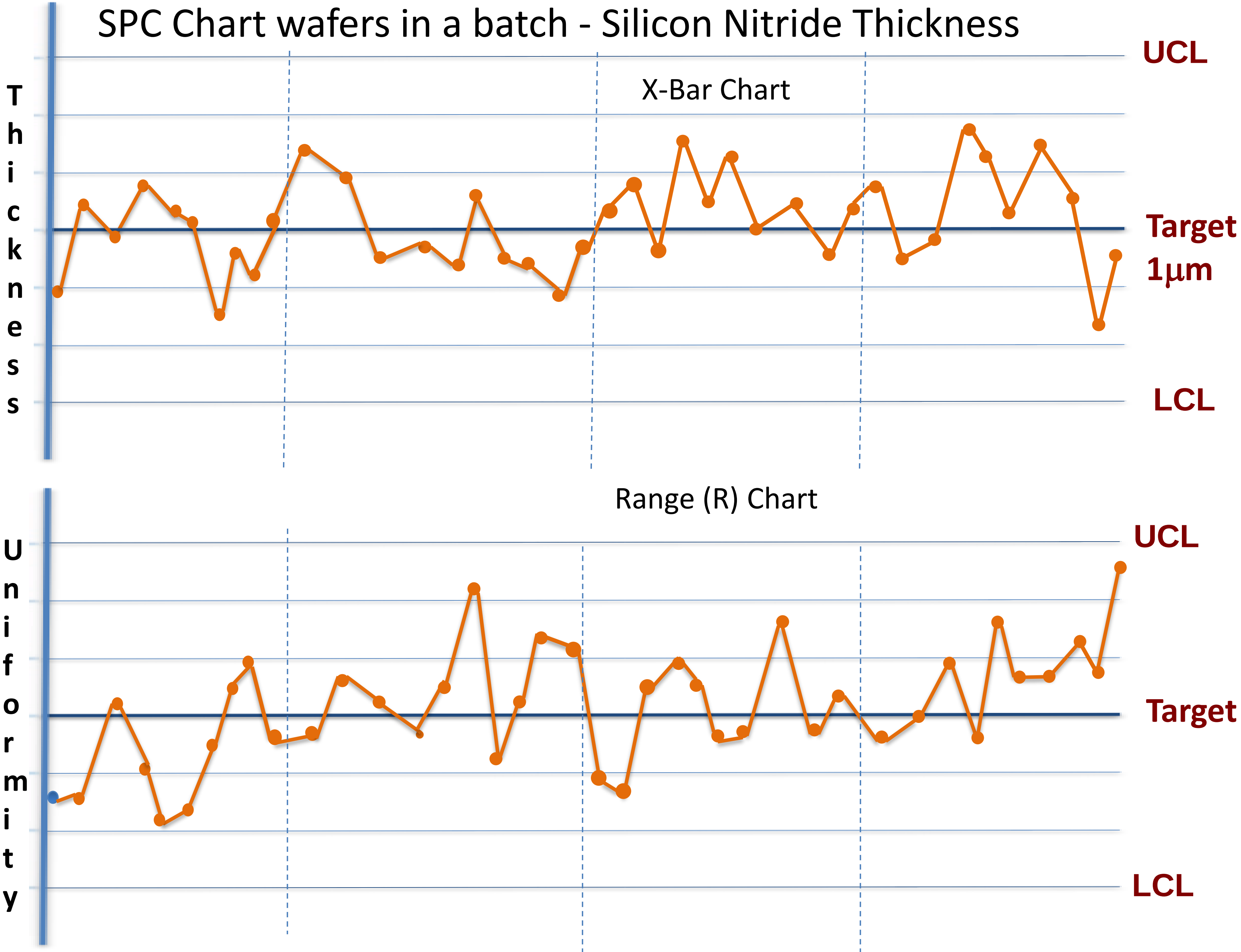
Environment

Contamination - particles

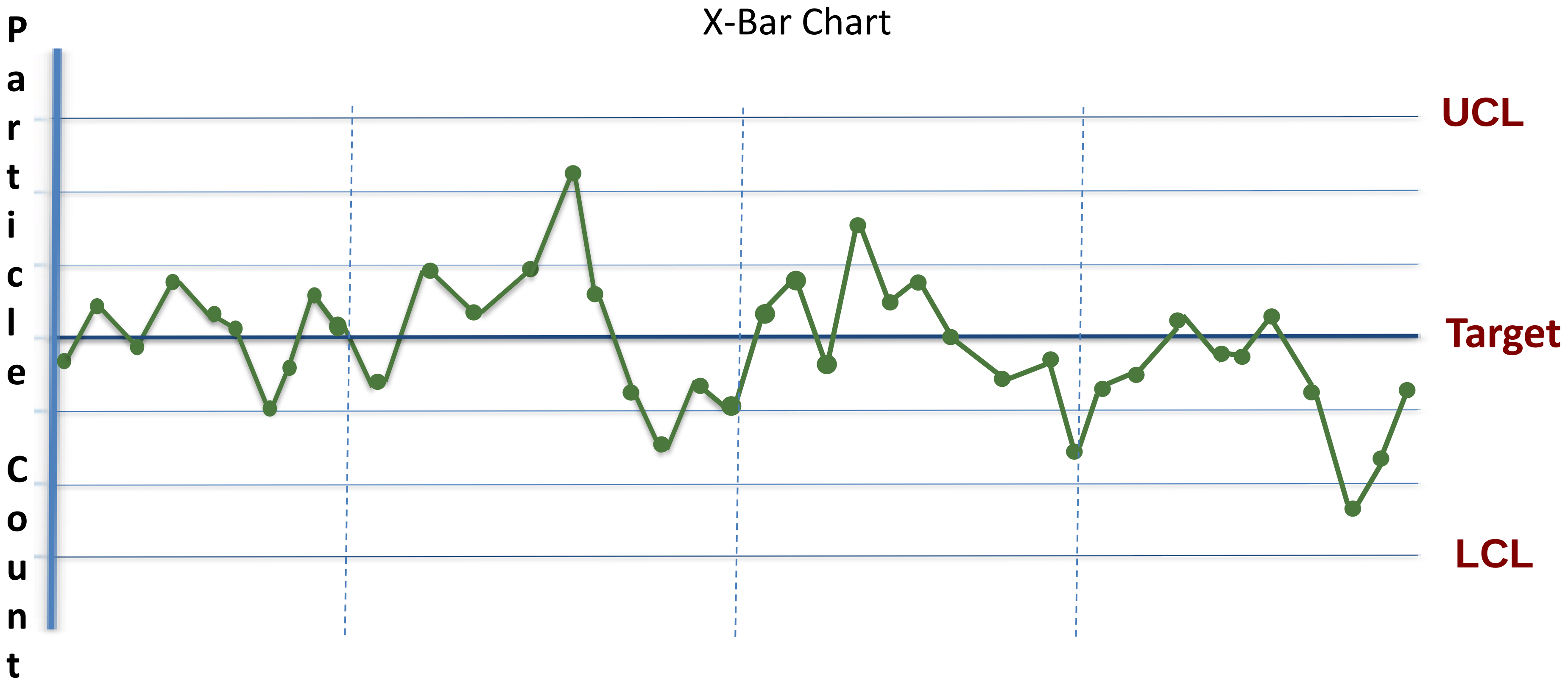
Now what do you want to see?

- Data Available to you
  - Thickness & Uniformity of metal SPC
  - Thickness & Uniformity of SiN SPC
  - KOH Etch Temperatures SPC
  - Particle count after Frontside Photolithography
  - Particle count after Lift-Off
  - Lift-off defective chart
  - Lift-off defect pareto

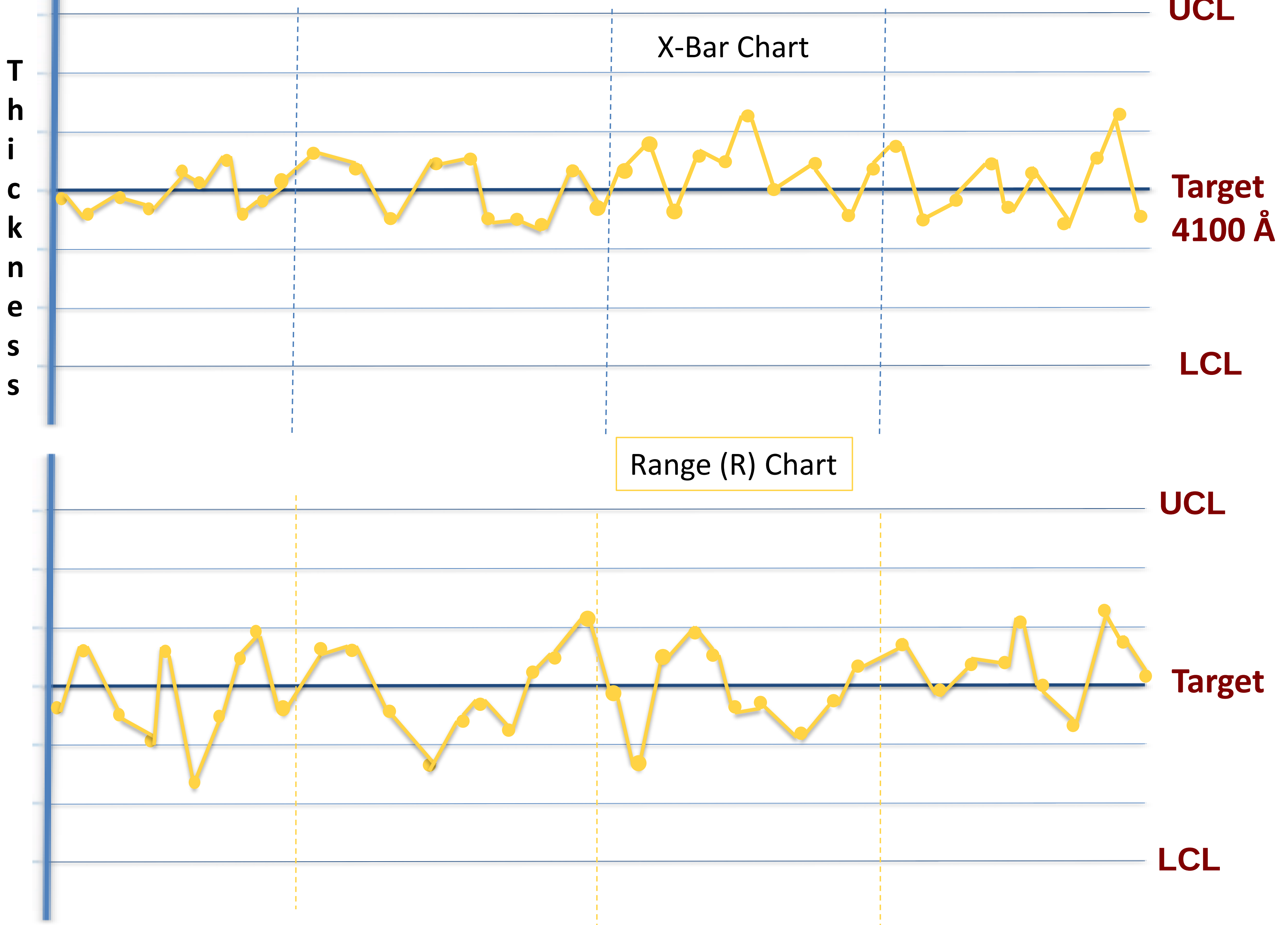
SPC Chart wafers in a batch - Silicon Nitride Thickness



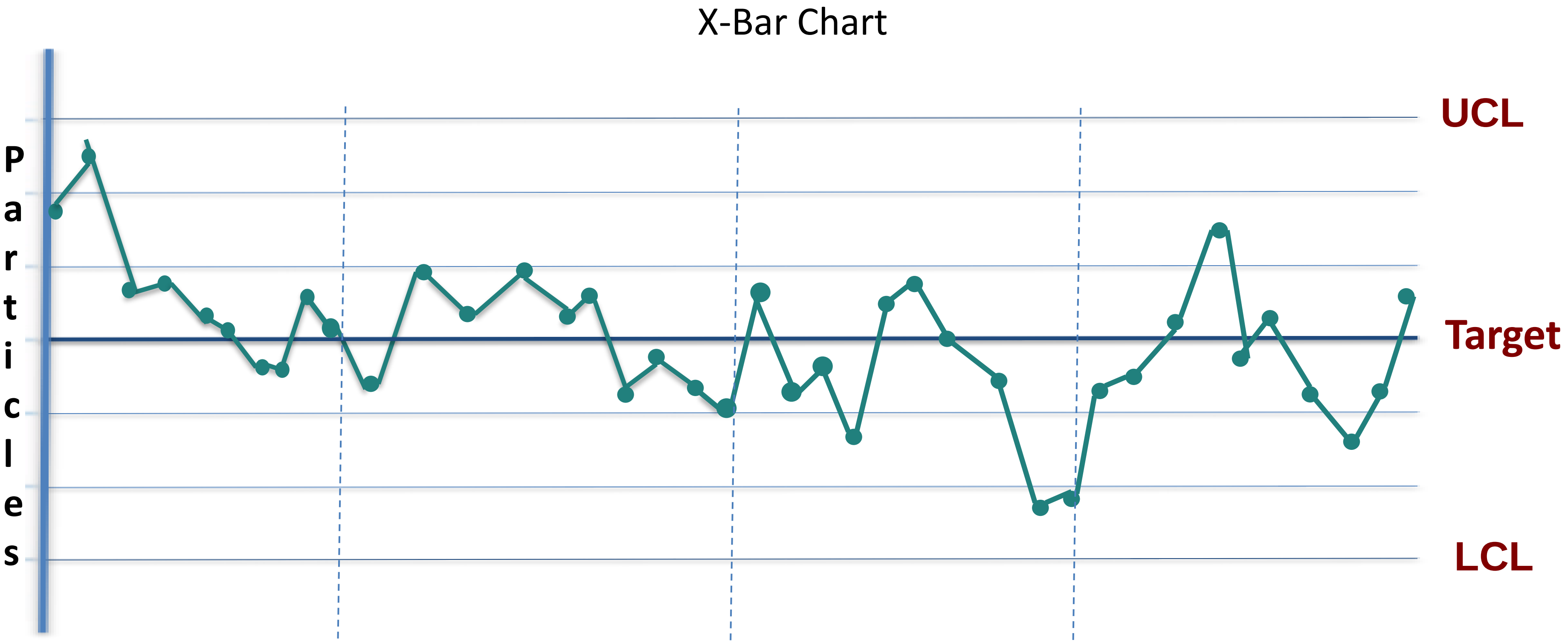
SPC Chart of Particle Count after Frontside Photolithography



SPC Chart wafers in a batch – Metal Thickness

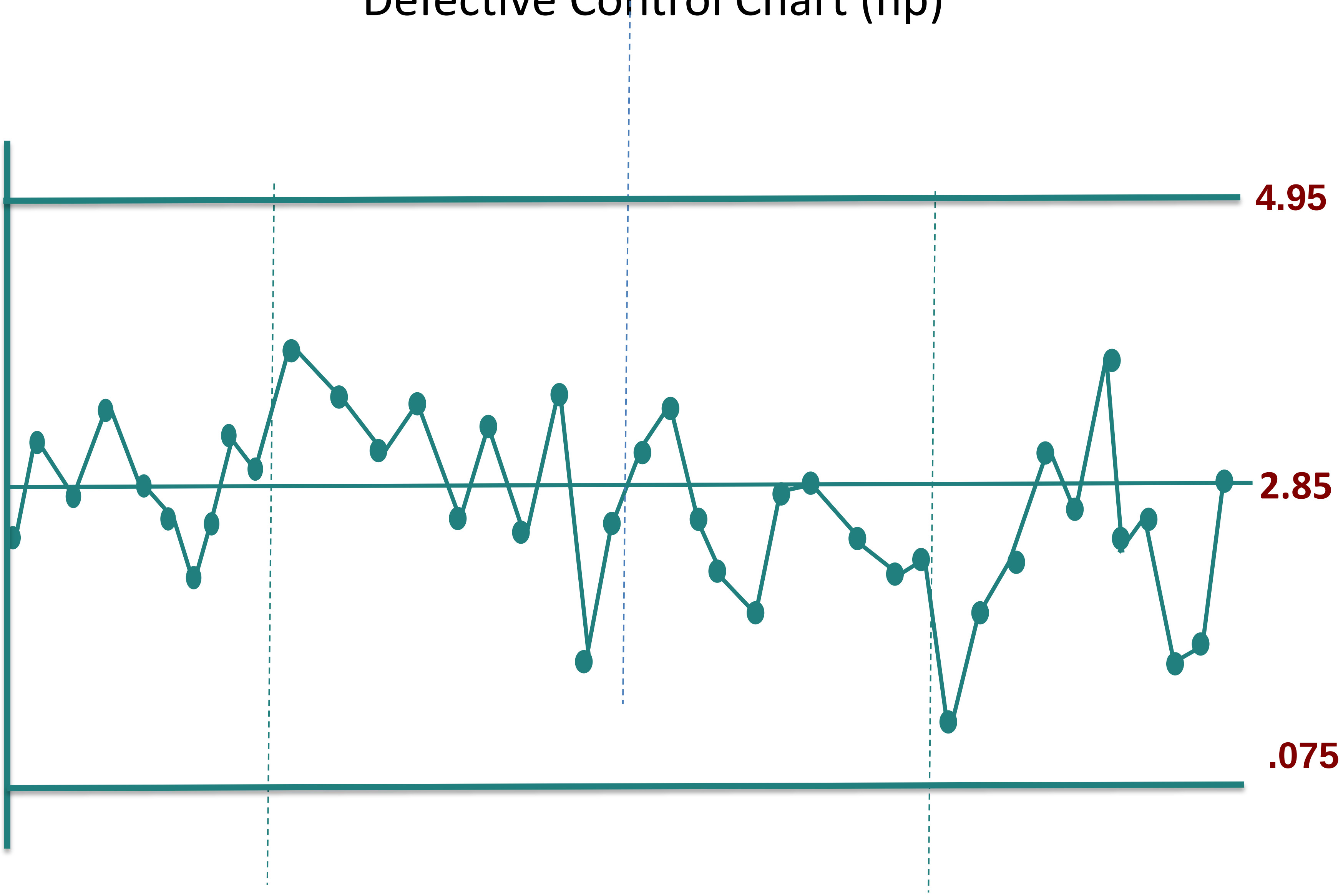


SPC Chart of Particle Count after Lift-Off

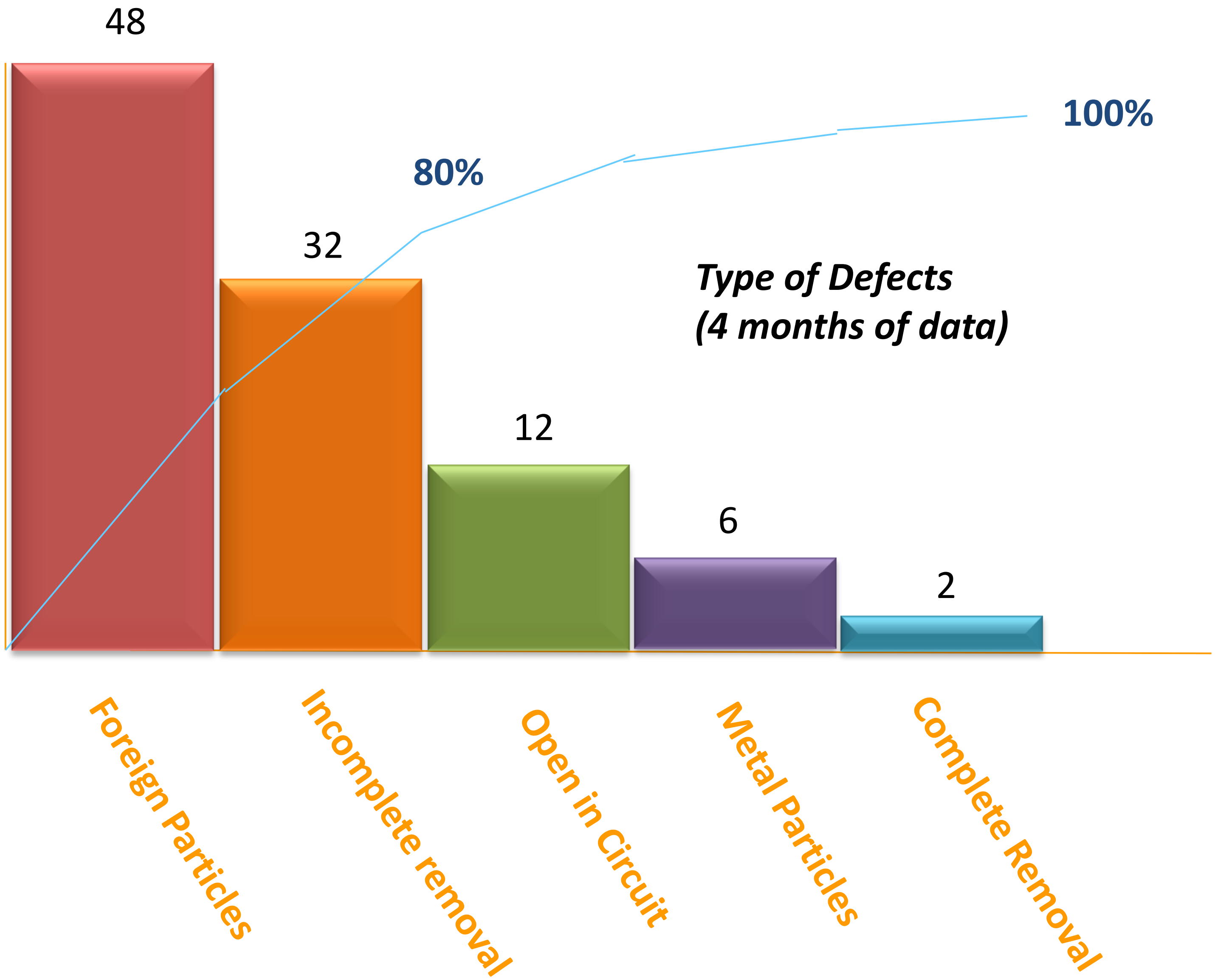


Lift-off Defective Chart

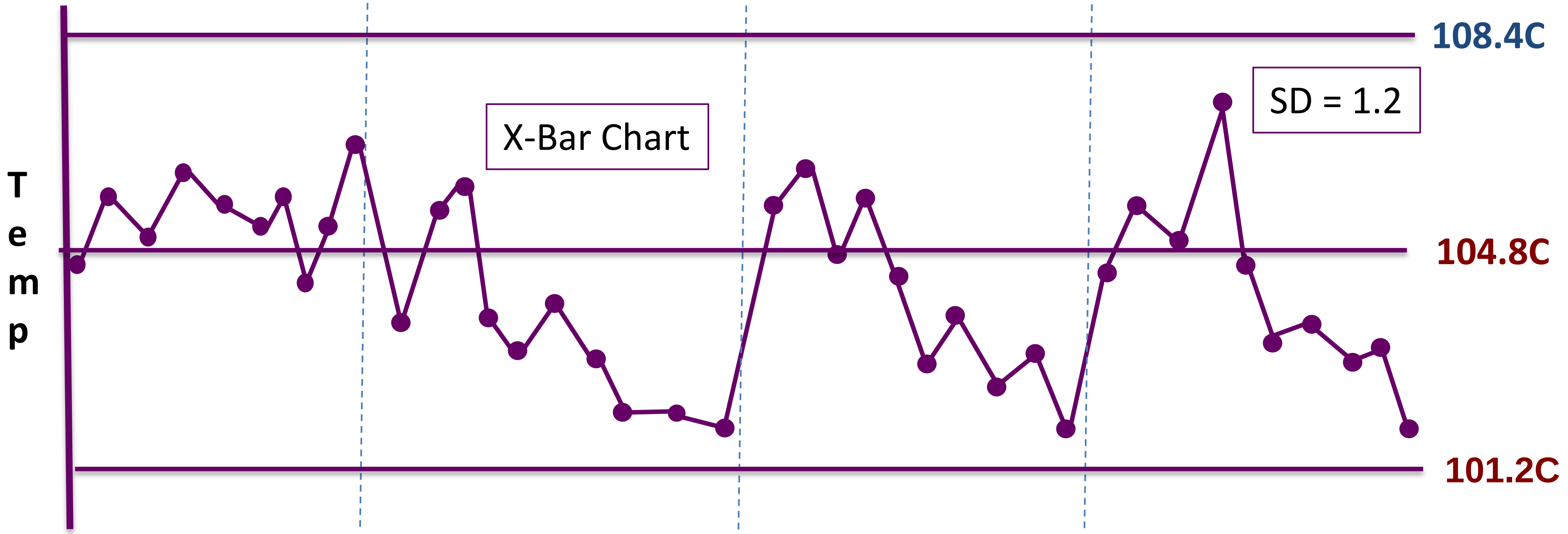
Defective Control Chart (np)

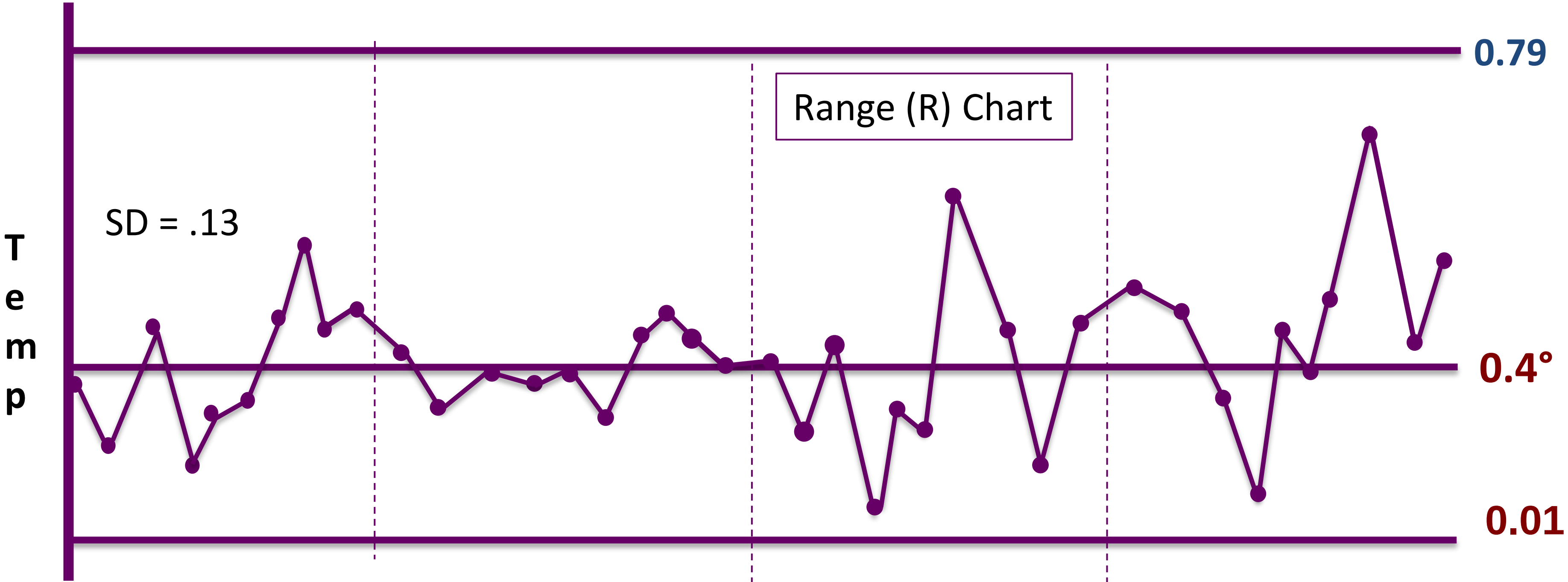


Lift-off Defects

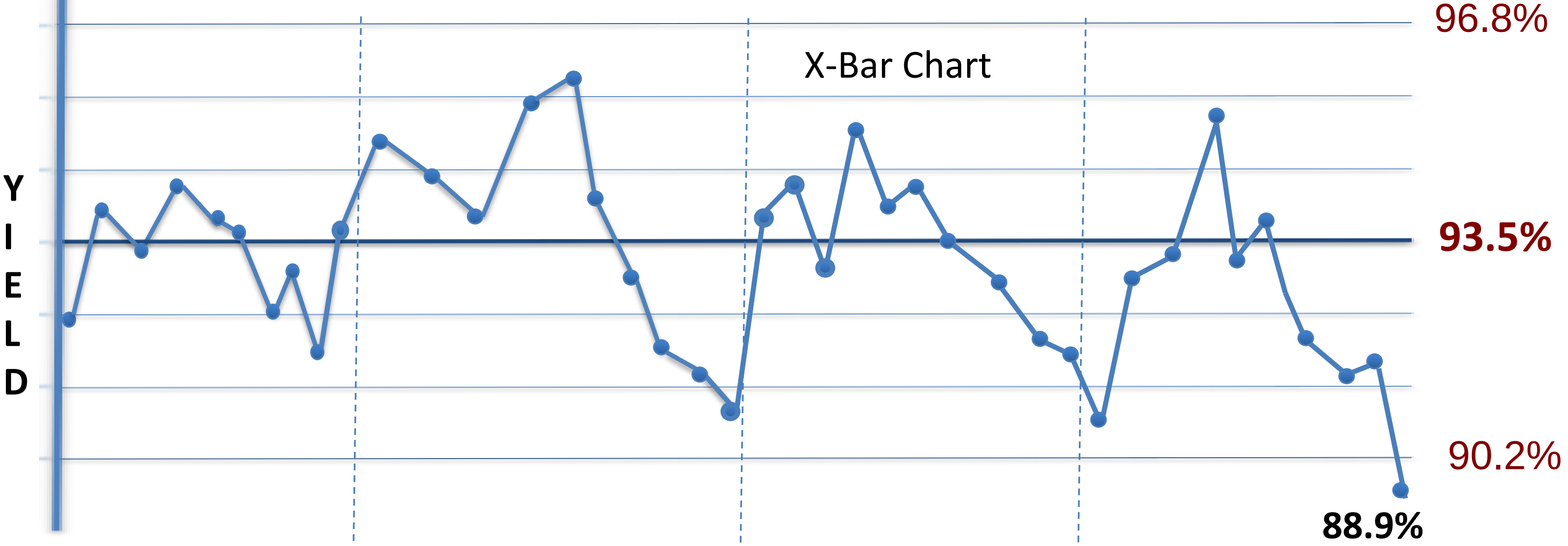


Temperatures for Initial KOH Etch @ 105 C for 2 hours

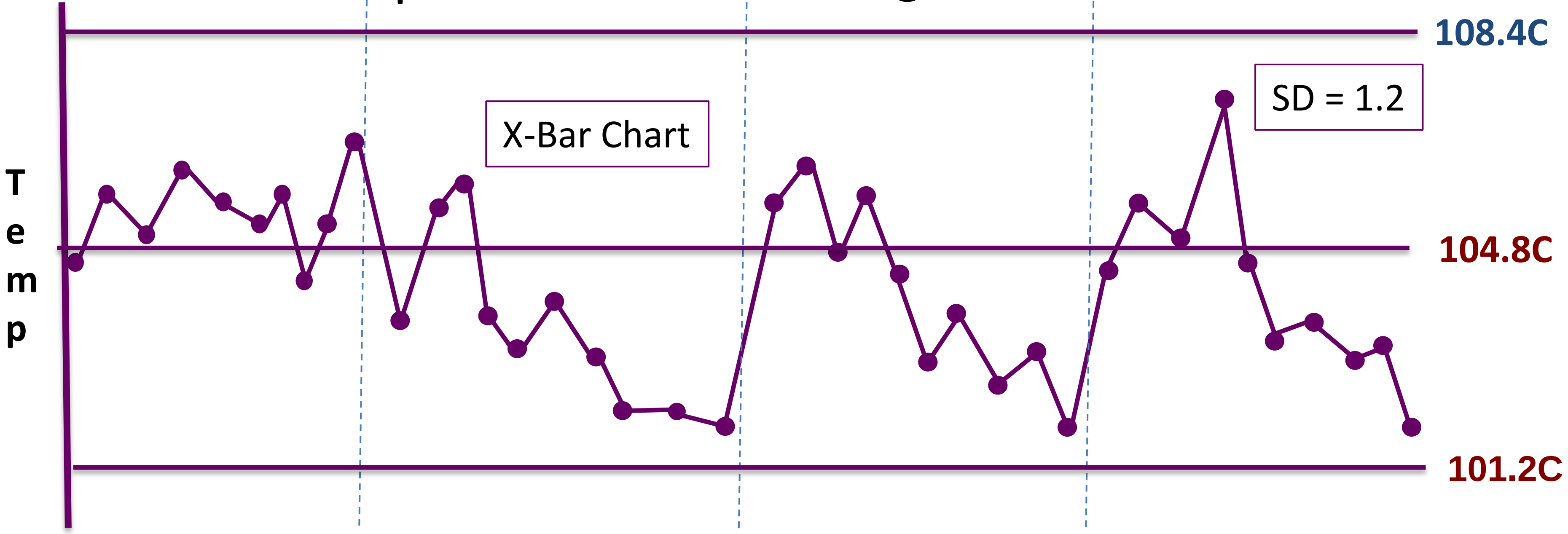


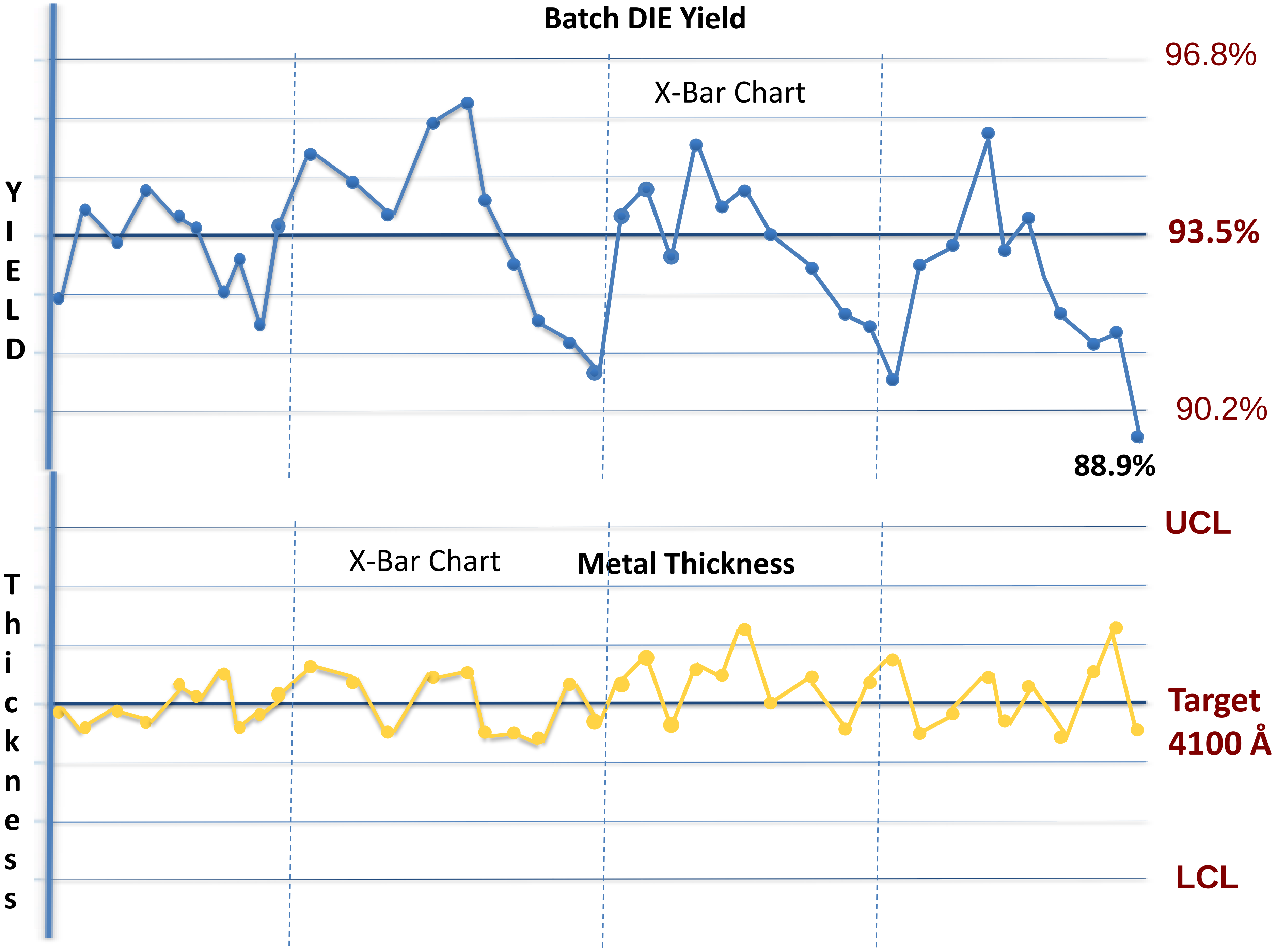


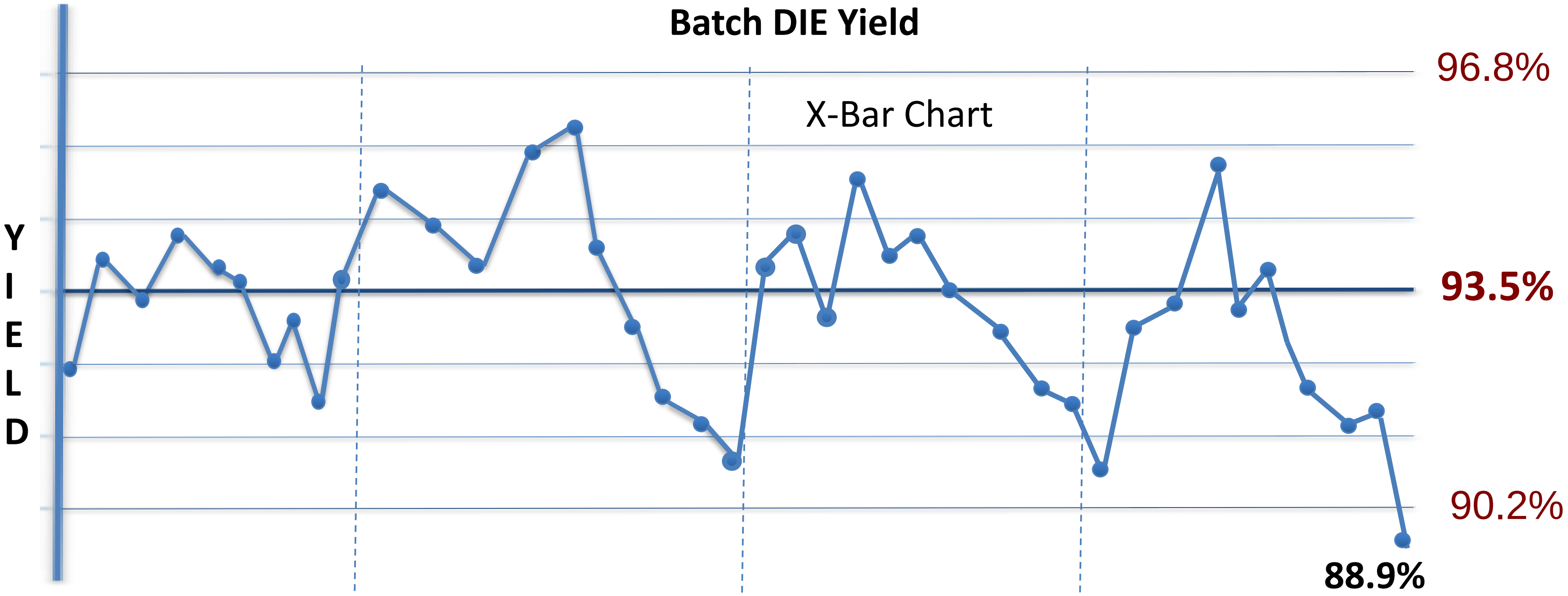
Batch DIE Yield



Temperatures for Initial KOH Etch @ 105 C for 2 hours

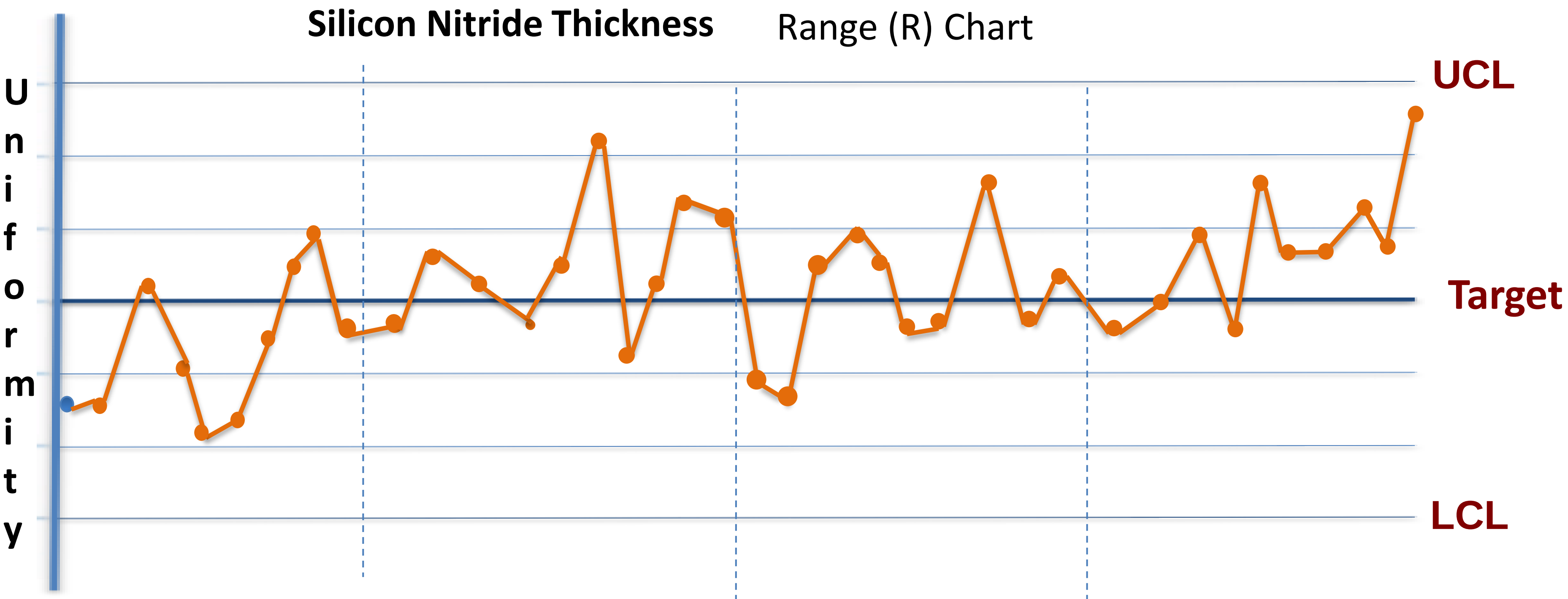



Batch DIE Yield
X-Bar Chart
YIELD
96.8%
93.5%
90.2%
88.9%
UCL
X-Bar Chart
Metal Thickness
Thickness
Target
4100 Å
LCL



Batch DIE Yield

X-Bar Chart



Silicon Nitride Thickness

Range (R) Chart

5. Develop an Action Plan

Recognize the a Problem Exists

Analyze the Problem

Identify Possible Causes

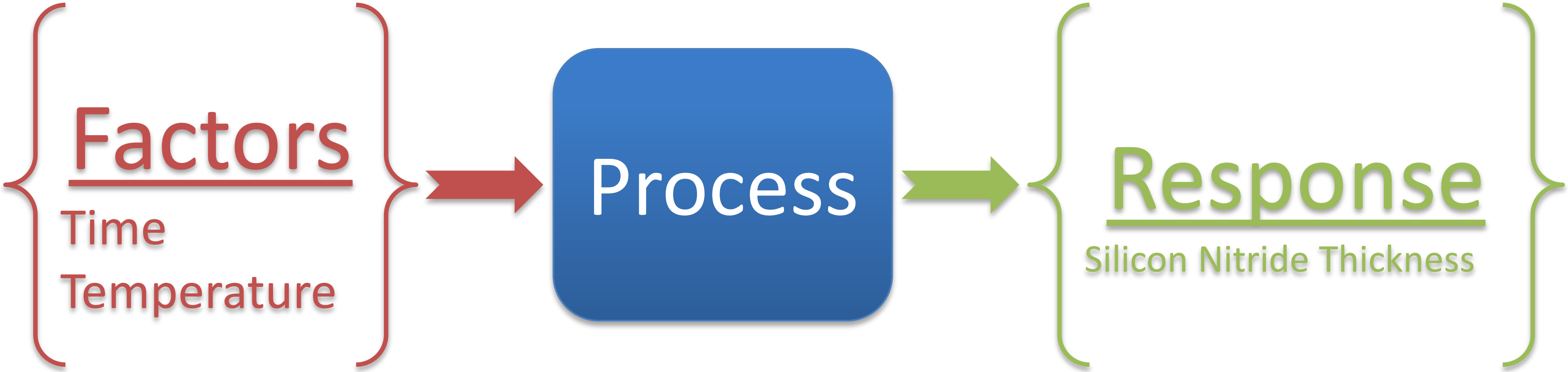
Evaluate Possible Causes

Develop an Action Plan

Verify and Record

5. Develop an Action Plan!

1. Correct the KOH Temperature Sensor Problem
2. Perform a DOE for the non-uniformity of the Silicon Nitride Deposition
   - 2^2 full factorial



Factors

Time

Temperature

Process

Response

Silicon Nitride Thickness

Factor Levels

6. Verify and Record

Recognize the a Problem Exists

Analyze the Problem

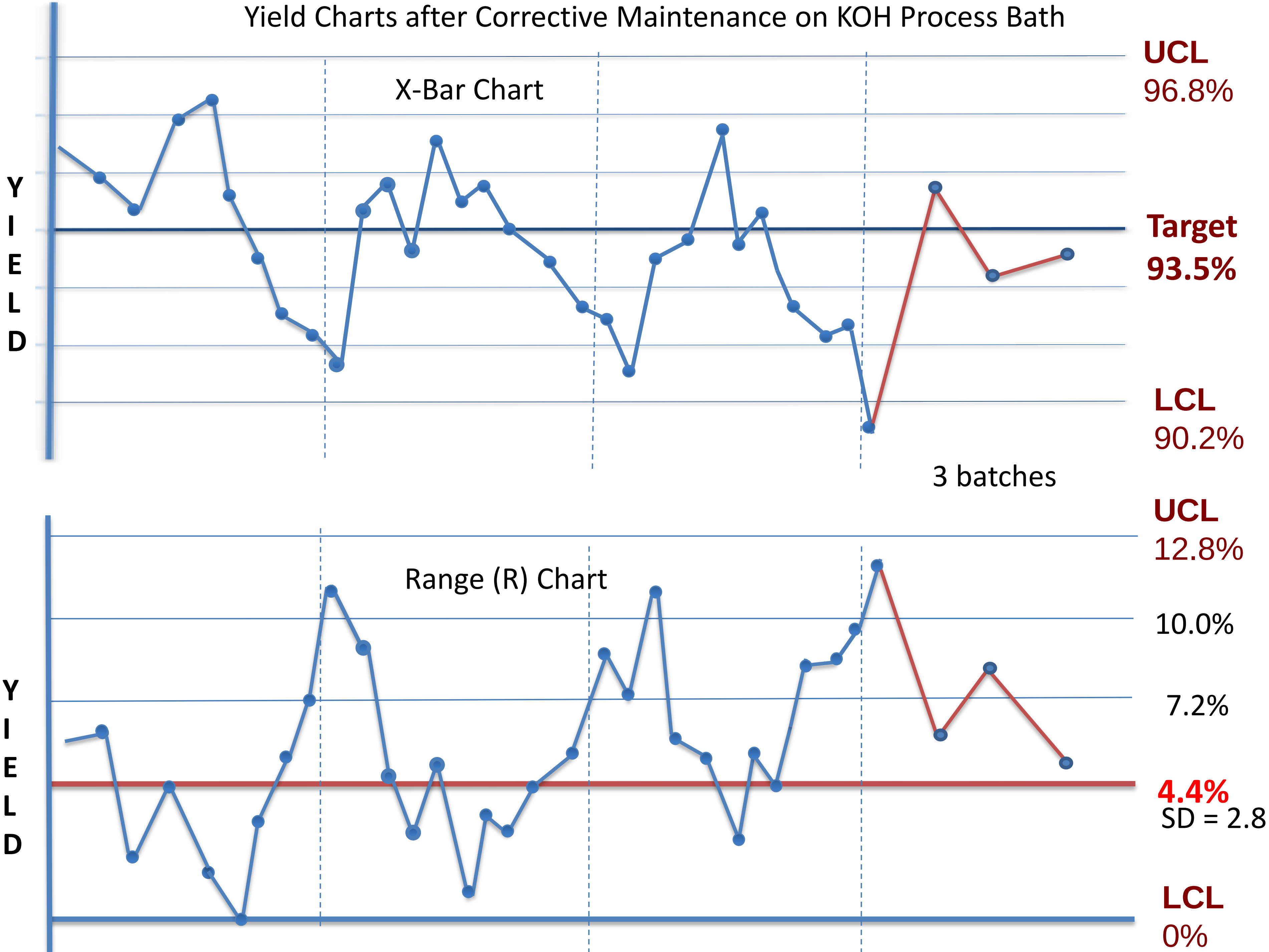
Identify Possible Causes

Evaluate Possible Causes

Develop an Action Plan

Verify and Record

Yield Charts after Corrective Maintenance on KOH Process Bath



Thank You
For Joining Us

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Webinar Resources

To access this webinar recording, slides, and handout, please visit

www.scme-nm.org

It was Fun!

Thank you for attending this SCME Webinar

Problem Solving Tools Applied to Microfabrication