ADC Specifications

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Important ADC Specifications

Even though designers of ADCs and engineers using ADCs must be familiar with literally dozens of specifications, only a few of these specifications are useful and relevant to the application. These are:

- Dynamic range
- Number of bits of resolution.
- Signal-to-noise ratio (SNR)
- Effective number of bits (ENOB).
- Spurious free dynamic range (SFDR).

Each of these will be reviewed briefly here except for resolution which was covered earlier in the module.

Dynamic Range

Dynamic range is the ratio of the largest signal to the smallest signal that an ADC can handle.

It is usually expressed in dB where dB = 20log (V_{max}/V_{min}).

Usually the maximum signal is represented by the maximum output code 2^N -1 and the minimum is the LSB or 1. Therefore,

$$dB = 20log(2^N -1/1)$$

For a 14-bit converter, the dynamic range is

$$dB = 20log(2^N -1) = 20log(16383) = 84.3 \text{ dB}.$$

Signal-to-Noise Ratio

Signal-to-noise ratio (SNR or S/N) is the ratio of the RMS signal voltage to the RMS noise voltage expressed in dB.
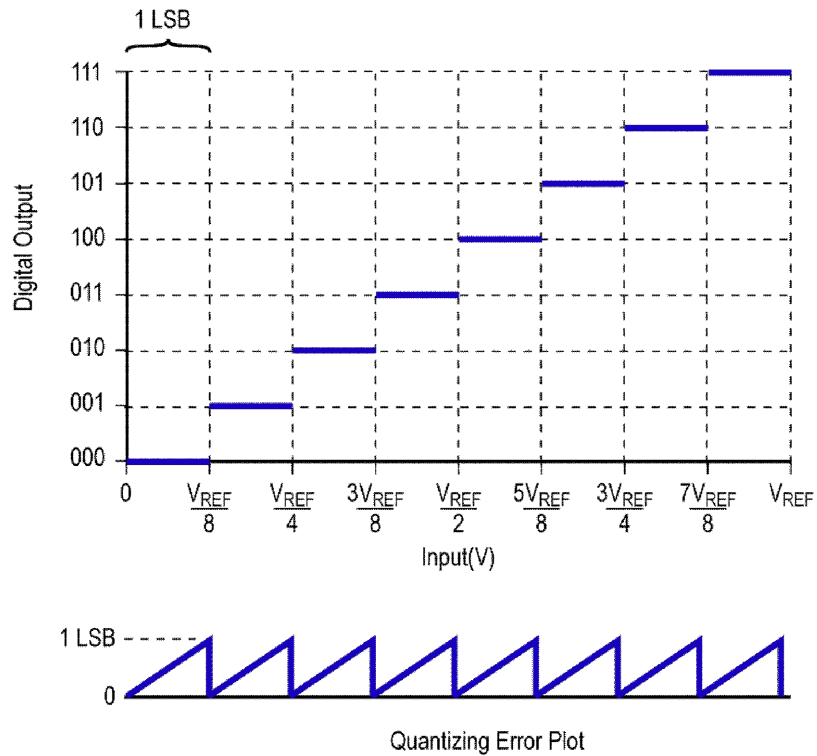
The main sources of noise are:

- Power supply ripple
- Clock
- External signals coupled into the circuit
- Quantizing noise
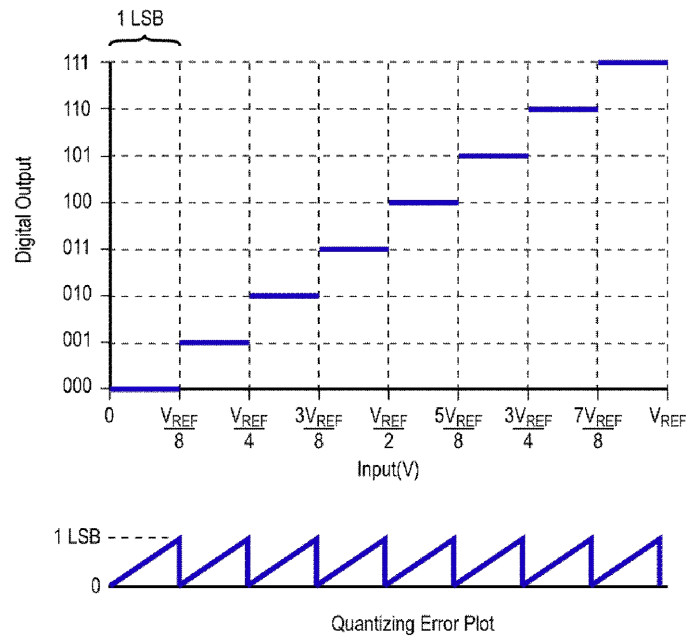
These problems are dealt with as follows:

- Good decoupling of the power supply with adequate bypass capacitors and in some cases inductors
- Routing clock line away from the ADC and reducing clock jitter
- Shielding the circuit or increasing distance to interfering sources
- Increasing resolution only way to quantizing noise

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Quantizing Noise

A discussion of this graphic is presented in the pages that follow. You can print this graphic for study purposes before going on.

Quantizing Noise

The input/output relationship of a simple 3-bit ADC is shown here. The V_{ref} is divided into $2^N = 2^3 = 8$ increments. The resolution is $V_{ref}/8$.
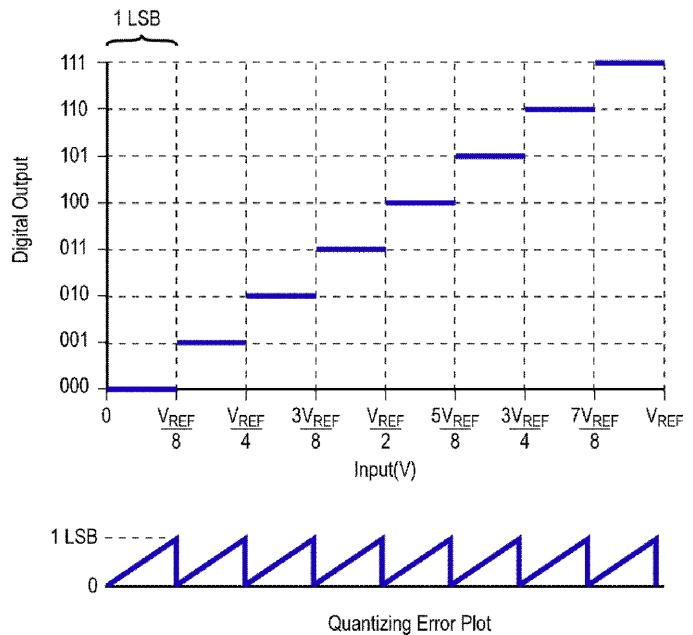
The plot at the bottom of the graph is the error expressed in units of 1 LSB of resolution.
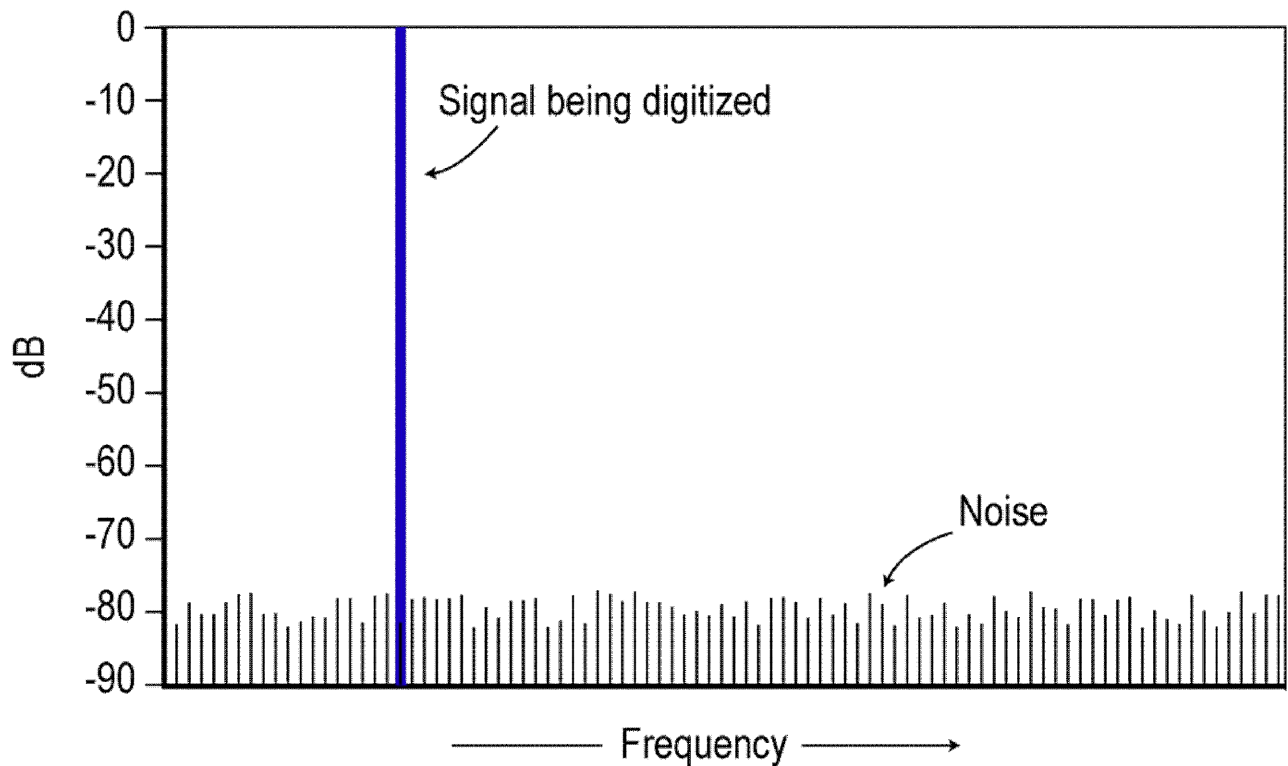
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Quantizing Noise

With the ADC input zero, the output code is 000. There is no error. However, with any analog input between zero and one LSB, there will be some error rising linearly from zero to one LSB.

There is an uncertainty in the output code when the input is between the ranges defined by the number of bits and the reference voltage. The maximum error is 1 LSB.

The quantizing error can be reduced by increasing the number of bits of resolution.

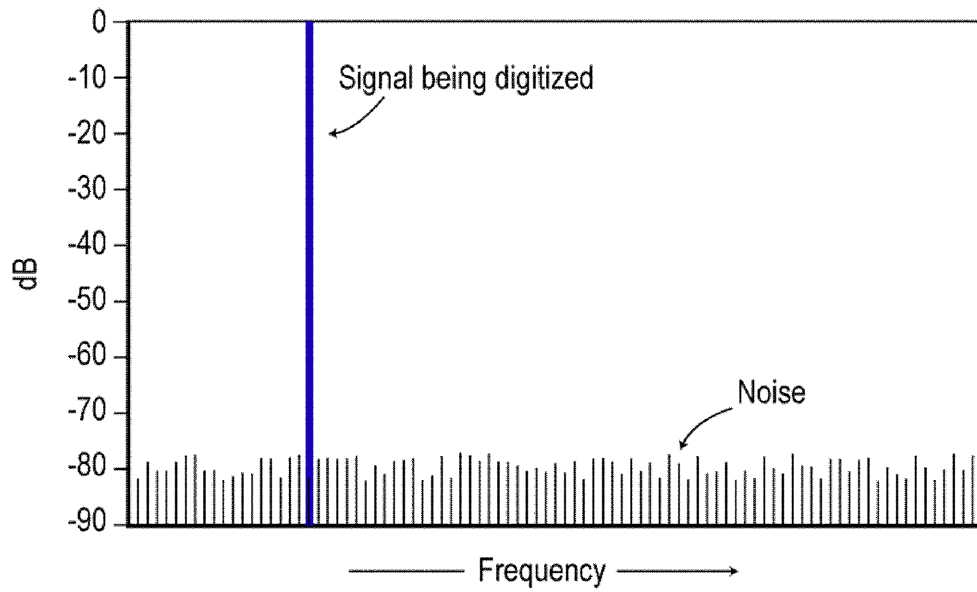Quantizing Error Plot

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Visualizing Quantizing Noise

A discussion of this graphic is presented in the pages that follow. You can print this graphic for study purposes before going on.
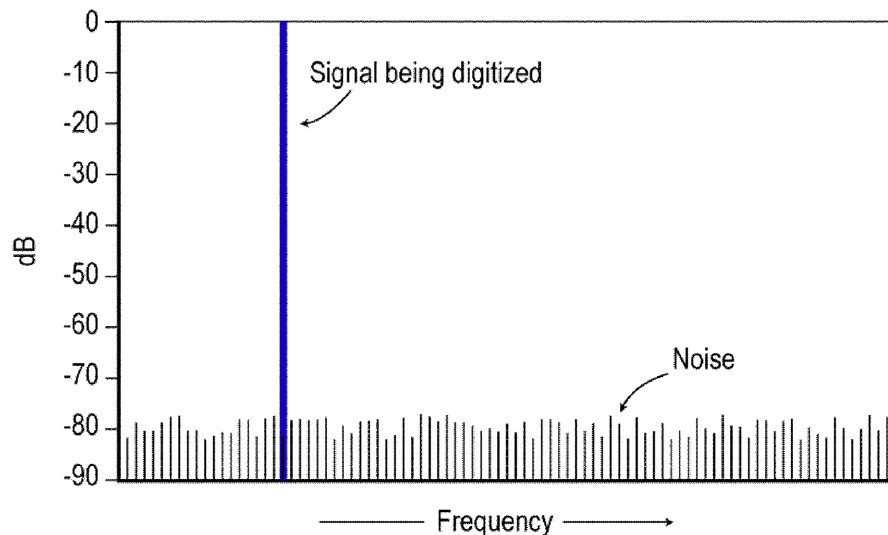
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Visualizing Quantizing Noise

If the binary output of the ADC is analyzed by the fast Fourier transform (FFT), the result is a frequency domain plot of the signal being converted and the noise, including quantizing noise.
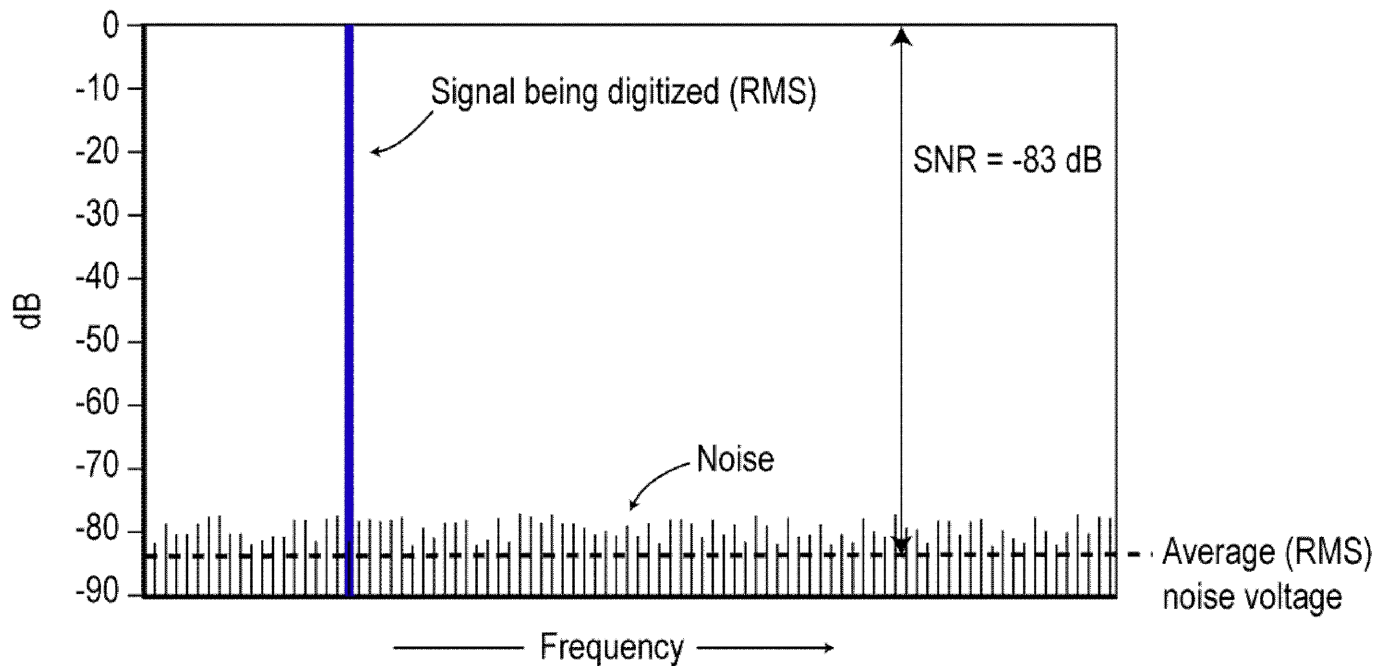
NOTE: For more information on the fast Fourier transform, see either the glossary or the WRE Fourier modules.
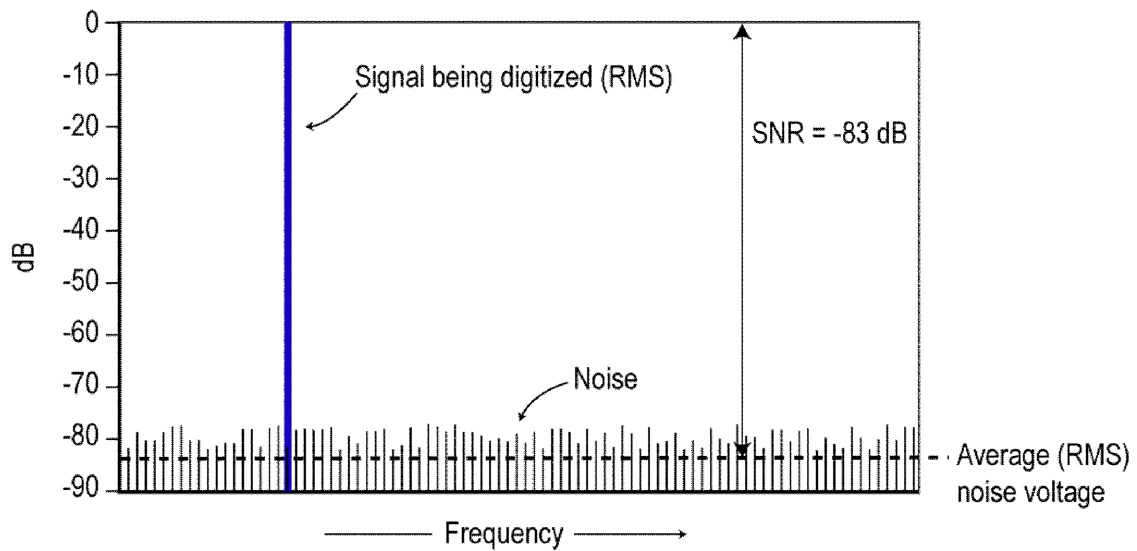
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Visualizing Quantizing Noise

In this frequency domain plot, the large signal vertical line represents a single frequency sine wave input being digitized. The smaller vertical lines represent the quantizing noise which is, in effect, the quantizing error frequency and the related harmonics resolved by the FFT. This is also the kind of plot that you would see if you took the binary data from the ADC and fed it to a DAC and viewed the DAC output on a spectrum analyzer. A high percentage of the noise is from quantization error.

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Visualizing SNR

A discussion of this graphic is presented in the pages that follow. You can print this graphic for study purposes before going on.

Visualizing SNR

This figure shows a similar plot where the noise components are random voltages from quantization noise and all other sources.

The average RMS value of noise is compared to the RMS value of the signal which is assigned the 0 dB level.

The noise is -83 dB below the signal level. The SNR is -83 dB.

Effective Number of Bits (ENOB)

ENOB is a specification that indicates that if the noise and harmonics are too large, they reduce the resolution. This means that the ADC in reality has fewer true bits of resolution.

ENOB is computed by knowing the SINAD value.

SINAD is the ratio of the signal amplitude and the amplitude of all the noise and distortion. Total harmonic distortion (THD) includes all of the harmonics. SINAD is expressed in dB.

SINAD for a perfect noise and distortion free ADC = 6.02N + 1.76 where N is the number of bits. The actual SINAD in a practical ADC will be less.
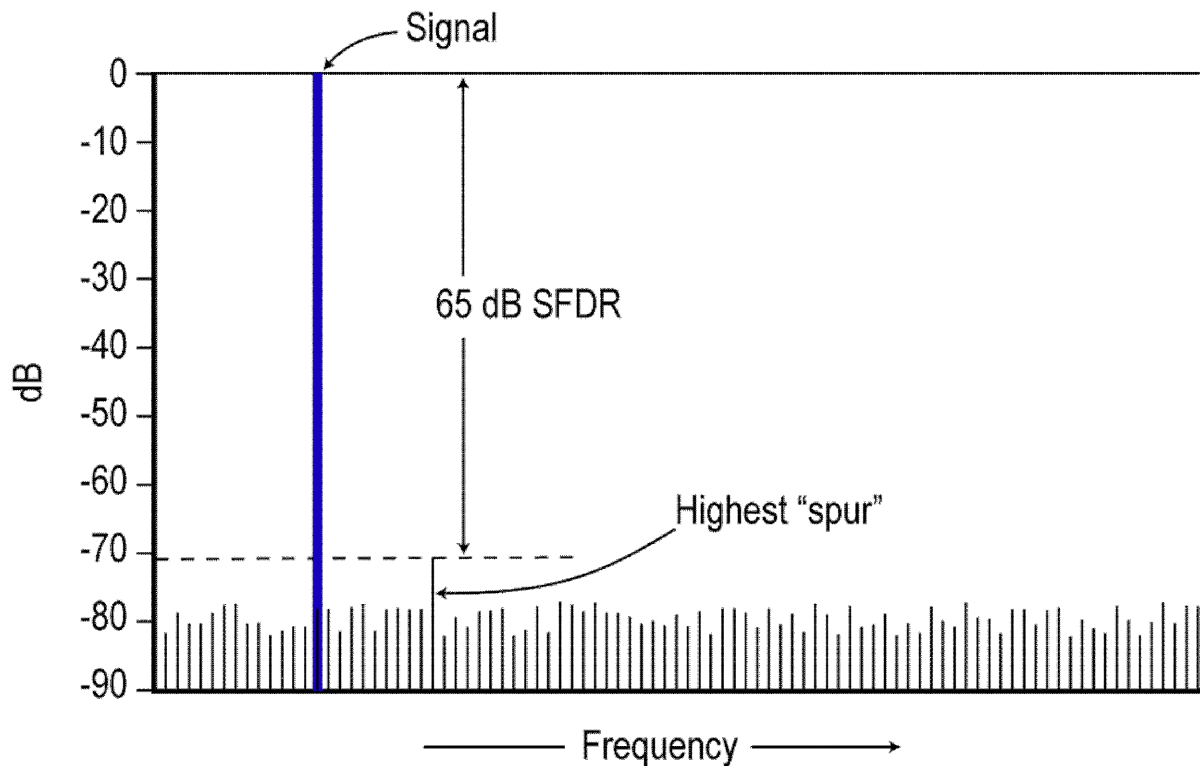
ENOB = (SINAD – 1.76)/6.02

Assume a 12-bit converter with a SINAD of 62 dB.

The ENOB is: (62 – 1.76)/6.02 = 10-bits.

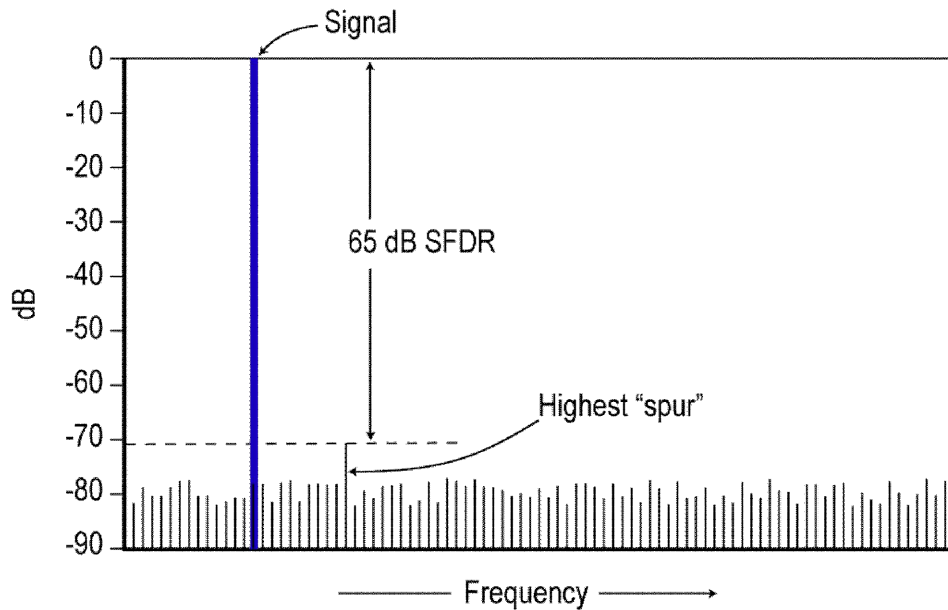This is equivalent of using a 10-bit ADC with no noise.

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Spurious Free Dynamic Range (SFDR)

A discussion of this graphic is presented in the pages that follow. You can print this graphic for study purposes before going on.

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Spurious Free Dynamic Range (SFDR)

The SFDR is the ratio between the RMS signal level and the highest amplitude spurious signal (spur).   A spur is an undesired signal that is not present in the input and whose source is sometimes not known.

SFDR is expressed in dB.

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Data Conversion Knowledge Probe 3
ADC Specifications

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