Types of Analog-to-Digital Converters

Popular Conversion Methods

There are many ways to convert an analog signal into a sequence of binary numbers but only a few are widely used.

The most common conversion approach is referred to as the successive approximations method.

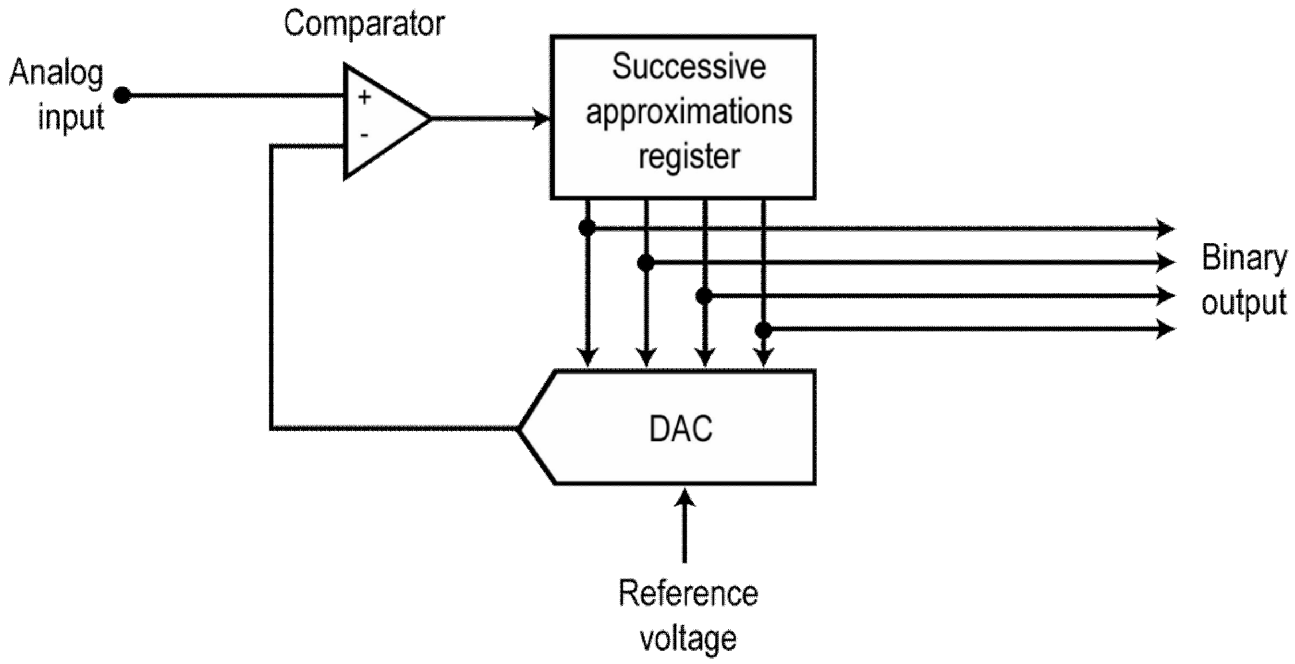
For conversion of very high analog frequencies, the flash method is used.

A version of the flash method called the pipelined approach is also popular for high frequency signals.

For audio applications, the sigma-delta method has become the most popular.

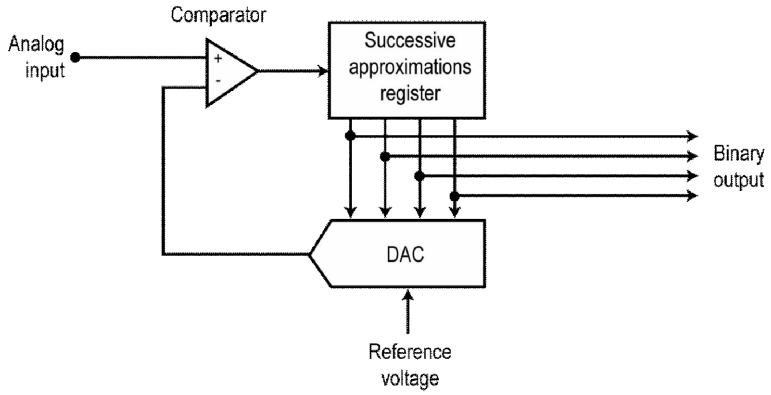
The dual slope method is used in test equipment and DC conversion where speed is not important. The dual slope method is not covered here.

Successive Approximations Converter



A discussion of this graphic is presented in the pages that follow. You can print this graphic for study purposes before going on.

Successive Approximations Converter

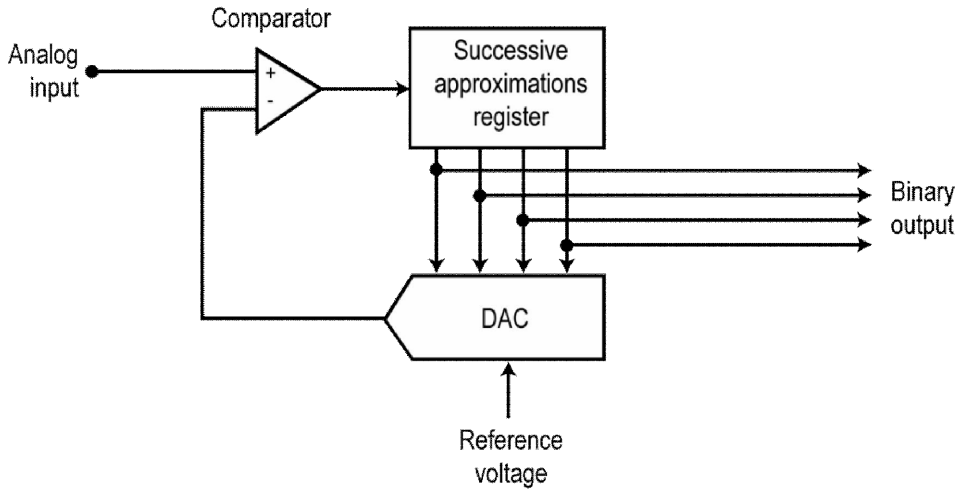


The successive approximations (SA) converter is by far the most widely used type. It is available in bit sizes from 8-bits to 16-bits in two bit increments.

The 4-bit converter basic SA circuit is shown to illustrate the principles of the SA converter.

The analog input to be digitized is fed to one input of a fast op amp comparator. The other input to the comparator comes from a DAC. If the analog input signal at the instant of sampling is greater than the DAC output, the comparator output is a binary 1. If the input is less than the DAC output, the comparator output is binary 0.

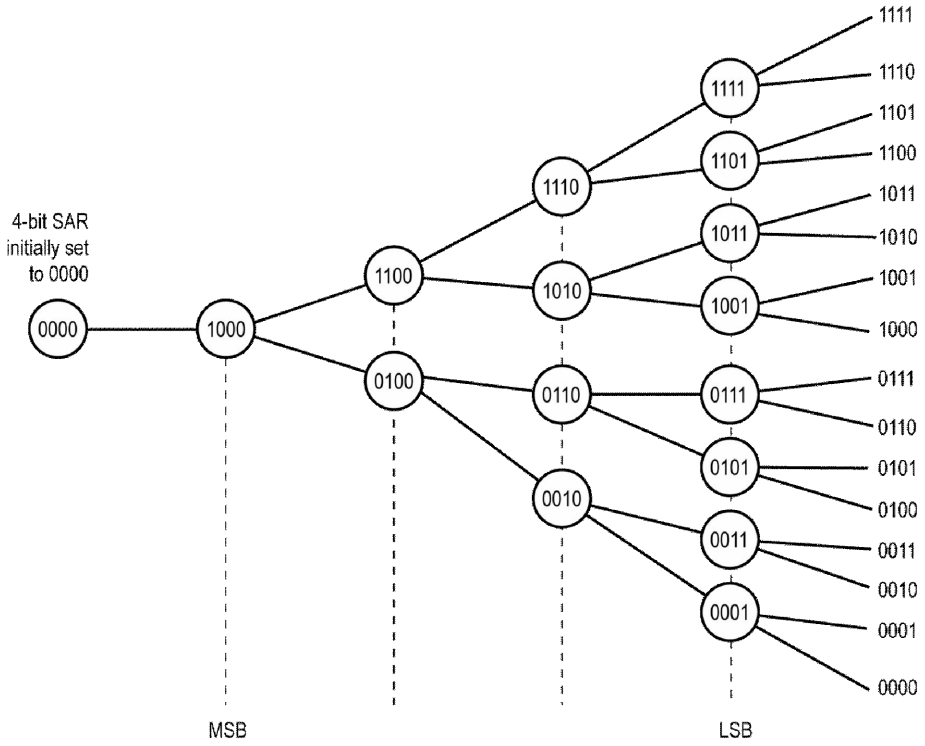
Successive Approximations Converter



The comparator output is fed to a special logic circuit called the successive approximations register (SAR). This is a collection of flip flops (one per bit) and logic gates that implement a unique algorithm for setting or resetting the flip flops.

The SAR flip flops form the ADC output which is also the input to the DAC.

SA Converter Operation



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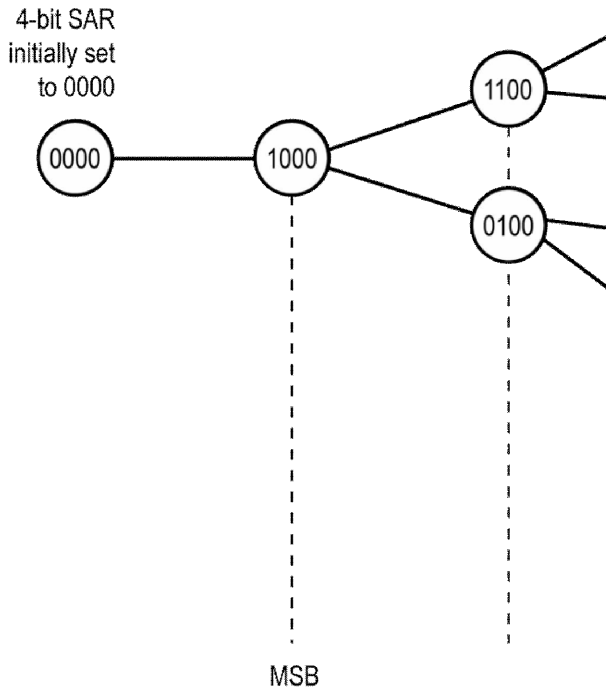
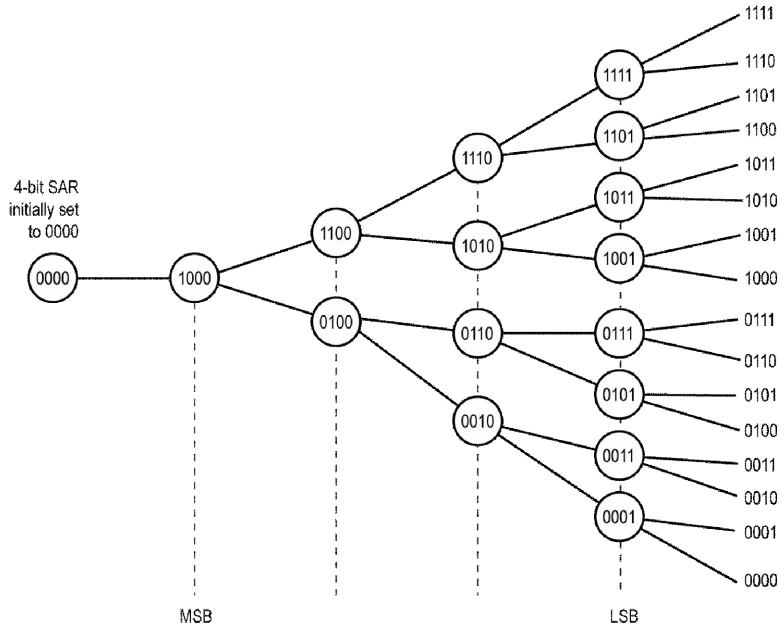
SA Converter Operation

In the algorithm implemented by the SAR, initially the SAR is set to 0000. The analog input signal is sampled and fed to the comparator. The analog value is compared to zero from the DAC. So the comparator output is 1. This signals the SAR logic, to set the MSB flip flop (FF).

With the MSB set, the SAR state is 1000 and the DAC output goes to one half the reference voltage value. That value is next compared to the analog input.



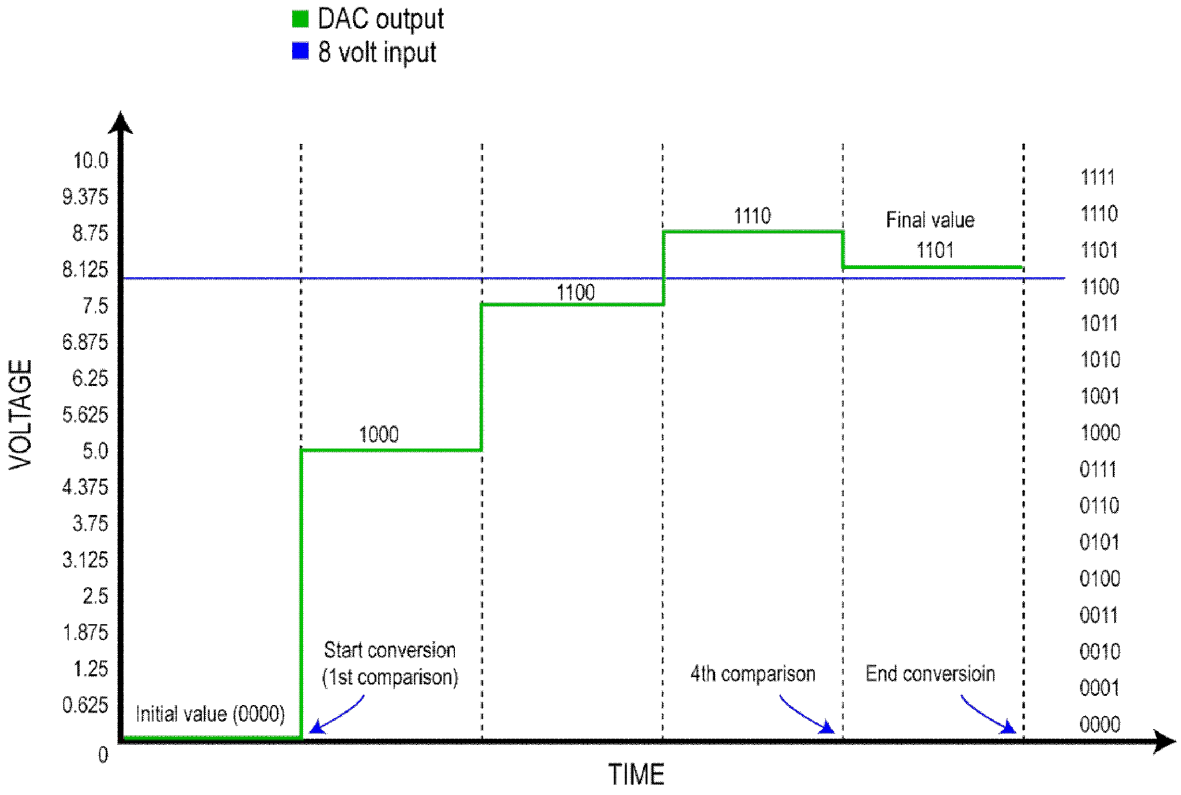
SA Converter Operation



If the analog input is still higher than the DAC output, the comparator output is binary 1 telling the SAR to set the next most significant bit.

However, if the analog input is less than the DAC output, the comparator output is a binary 0 which tells the SAR to turn off the MSB and set the next most significant bit. The comparison then continues in this way.

SA Converter Operation



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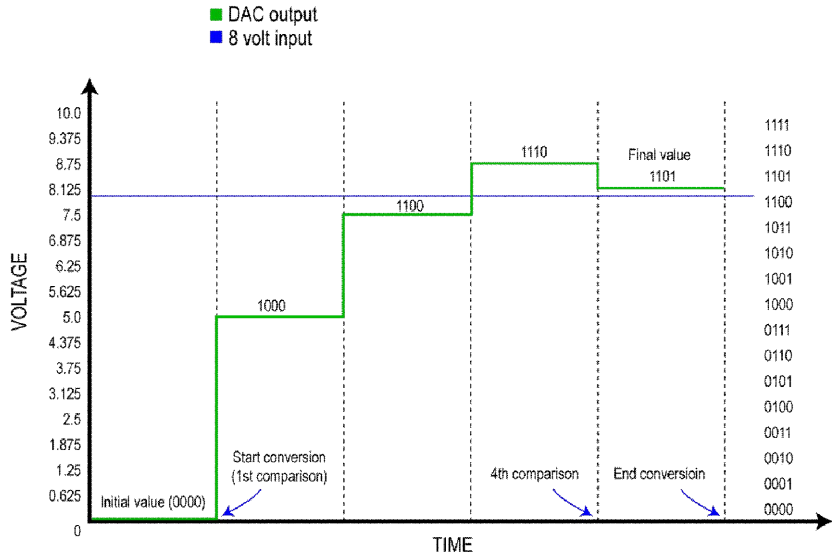
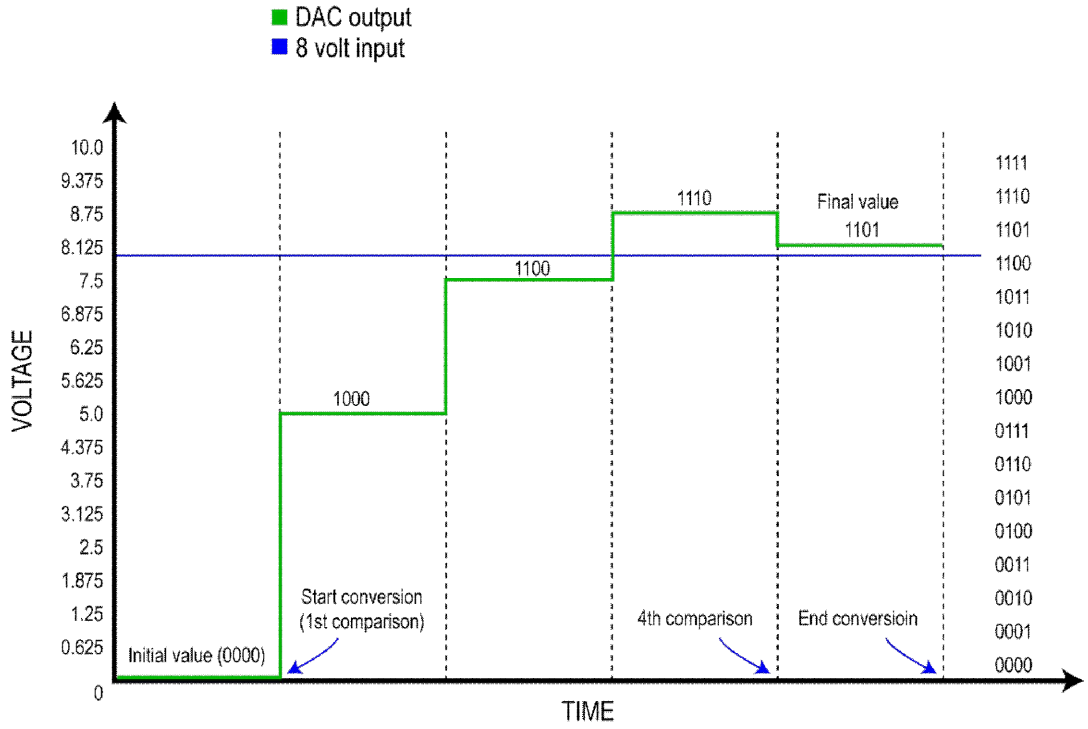
SA Converter Operation



The SA converter tests each of the bits from the MSB to the LSB one at a time. It uses the comparator to indicate if the analog input is less than or more than the DAC output.

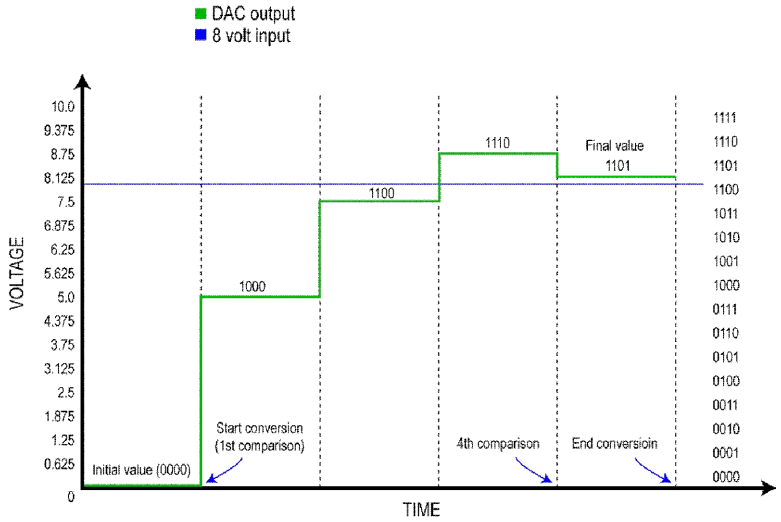
As the bits are turned off and on, the DAC output gets closer and closer to the actual value of the input. Ideally, the DAC output will equal the analog sample value upon completion of the conversion. In practice, it will actually only be within one LSB resolution.

SA Converter Operation



The figure shows a 10 volt reference on the DAC and a steady 8 volts DC input. With 4-bits there are 16 increments. The DAC output increments are 10/16 = 0.625 volts from 0.625 (0001) to 9.375 (1111).

SA Converter Operation



Turning on the MSB gives a code of 1000 sending the DAC output to 5 volts. This is less than the 8 volt input so the next most significant bit is turned on (1100). Again, the DAC output is less than the 8 volt input so the next bit is turned on (1110). The DAC output is now 8.75 volts or more than the input so the last bit is now reset to 0 and the next bit is turned on (1101). That is the fourth and last comparison so the conversion is complete. The output is 1101 or equivalent to 8.125 volts. This is within the ±1 LSB of the actual input of 8 volts.

Facts about the SA Converter

The SA converter makes the same number of comparisons as there are output bits. For N bits there are N comparisons.

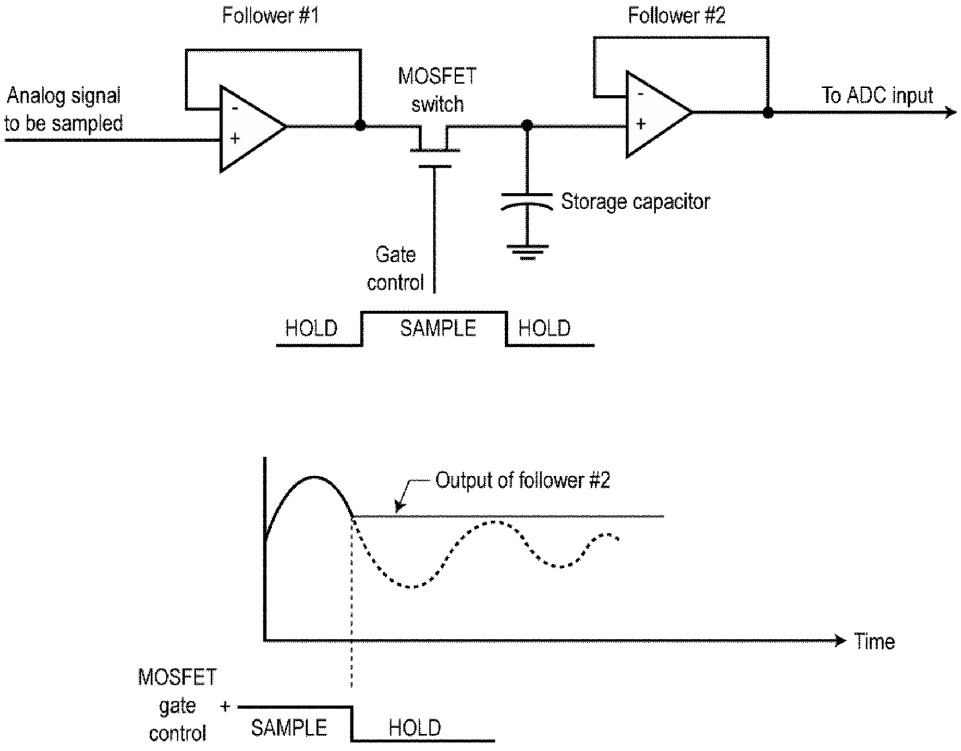
The conversion time is made up of the time that it takes to make the N comparisons. It is a function of the comparator switching speed, the settling time, and the logic circuit propagation delays. Conversion time is usually clocked by an external clock signal.

Conversion rates are typically less than 1 MHz but faster SA converters can achieve rates up to 2 to 5 MHz.

During the time it takes to make a conversion, the analog input signal may change because of the higher frequency components. This leads to an error referred to as aperture error.

To eliminate aperture error, the analog signal is usually sampled with a circuit called a sample/hold amplifier.

Sample/Hold Amplifier



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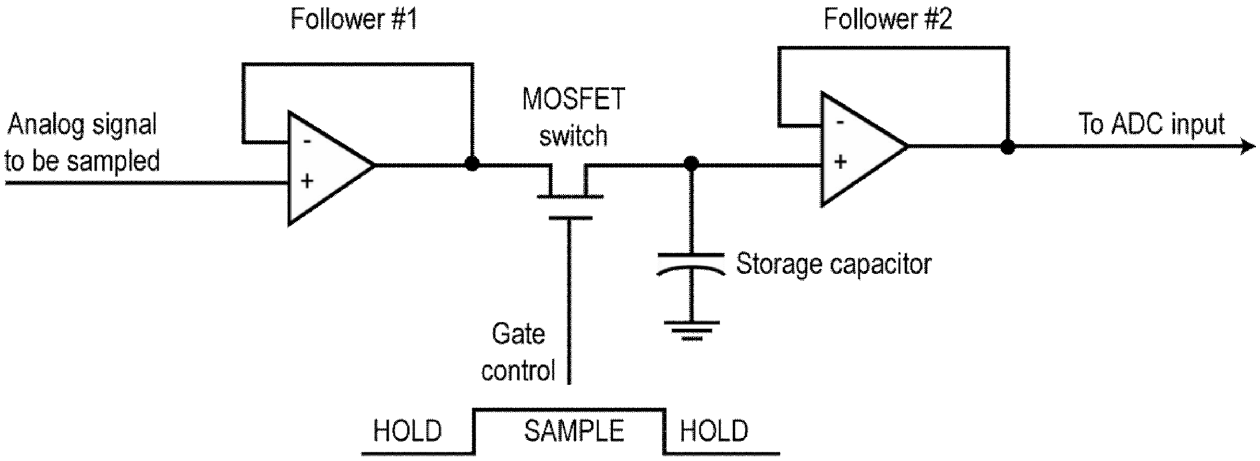
Sample/Hold Amplifier



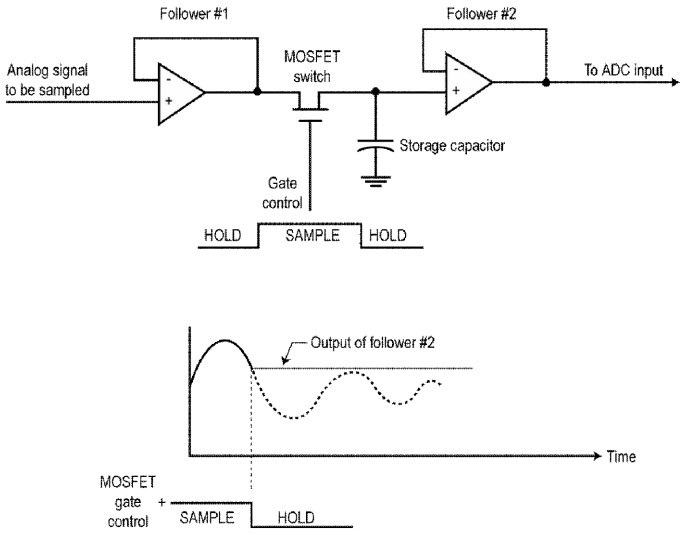
The sample/hold (S/H) amplifier is simply an input op amp follower with a very high input impedance, a fast MOSFET switch, a storage capacitor, and an output follower.

Normally, the MOSFET switch is on so the analog input signal simply charges and discharges the capacitor directly. The op amp output follows, or tracks, the analog signal.

Sample/Hold Amplifier

To sample the analog signal, the MOSFET is switched off by a logic signal. At the instant the MOSFET is turned off, the analog input voltage level is stored on the capacitor. The follower #2 output is the sample value that is applied to the AD converter input. The very high input impedance of follower #2 does not discharge the capacitor to any serious extent so the sample value remains constant during the conversion.

The S/H amplifier is sometimes referred to as a track/store (T/S) amplifier.



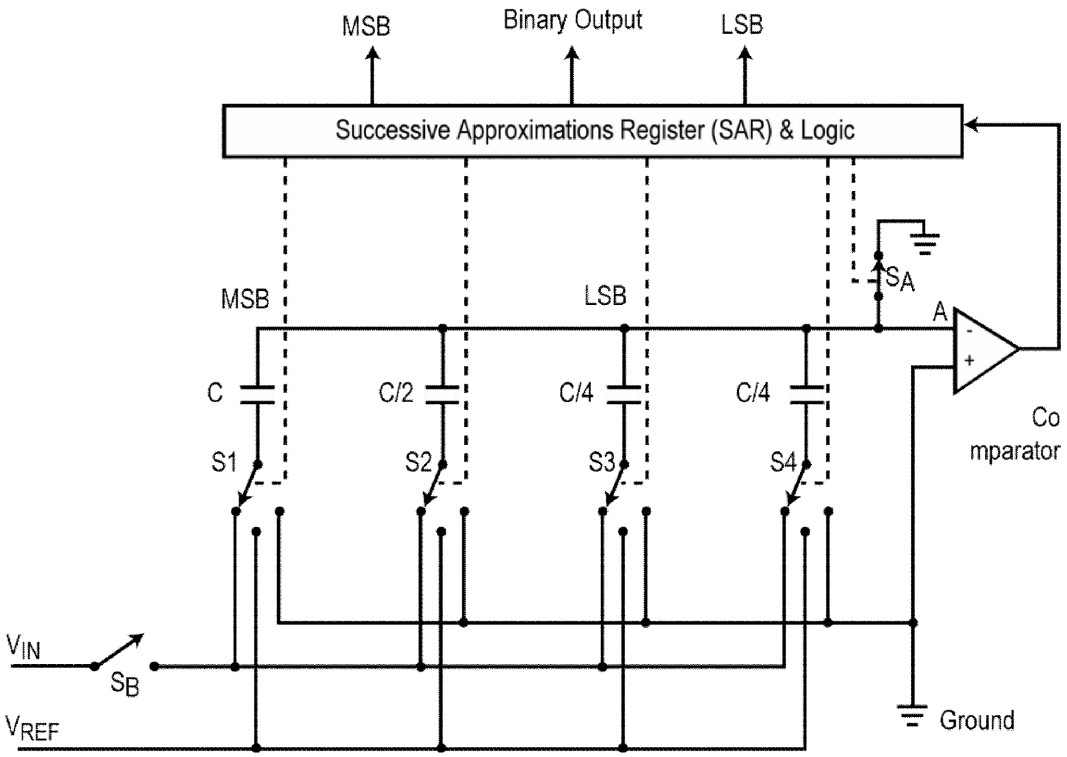
Capacitor Storage Array SA Converter

The earlier R-2R type DAC SA converters used took up considerable chip space on an integrated circuit and required special laser trimming during manufacture to ensure precision and monotinicity.

Newer SA ADCs use a switched capacitor array DAC to save chip space, improve conversion speed, and to eliminate the separate S/H amplifier required.

Such switched capacitor SA ADCs are so small they can be easily integrated into other larger circuits such as an embedded controller.

Switched Capacitor SA ADC



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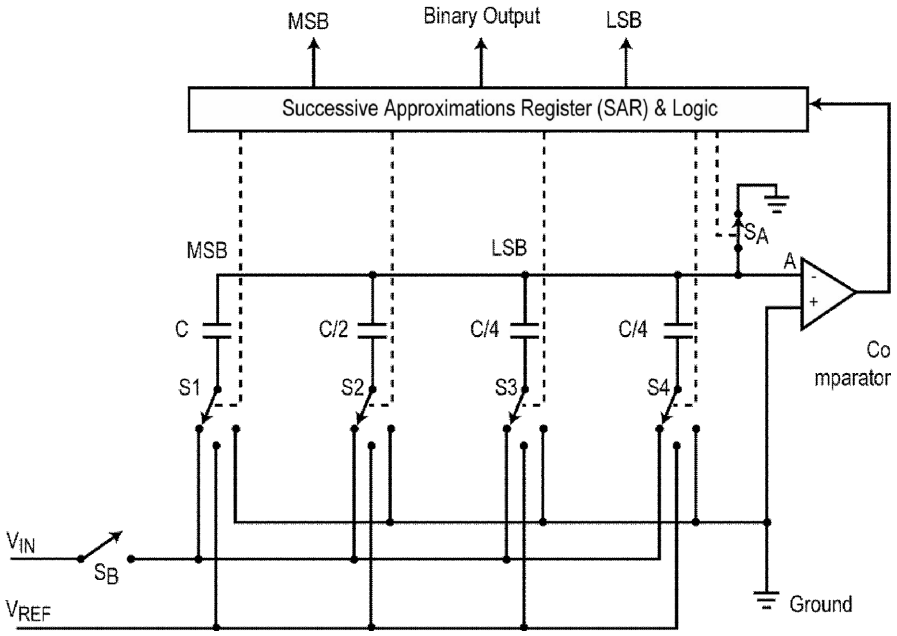
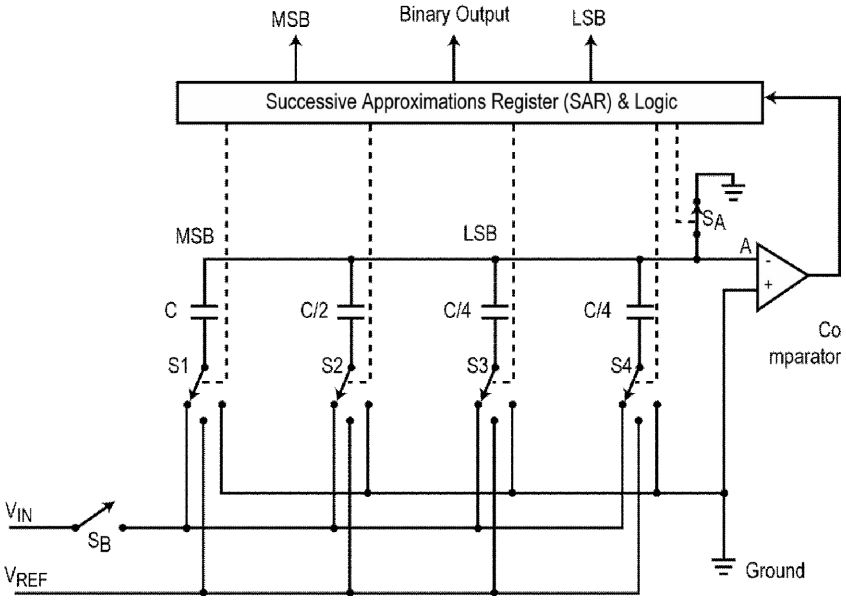
Switched Capacitor SA ADC



This is a simple 3-bit switched capacitor ADC. It implements the successive approximations algorithm by testing each bit in sequence from the MSB to the LSB.

The comparator is a high speed op amp where a portion of the analog input sample is compared to ground.

Switched Capacitor SA ADC

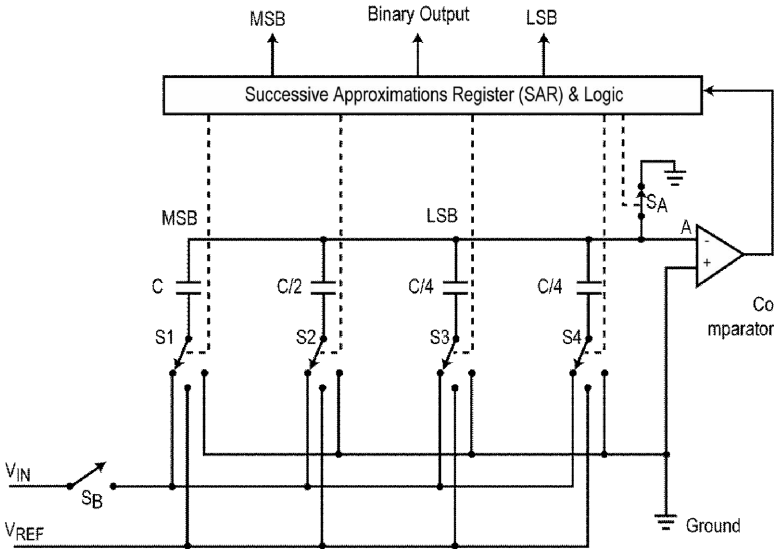


The capacitors form a storage cell for the analog sample so no external S/H amplifier is needed.

The capacitors are binary weighted (C, C/2,C/4) where the weight of one is twice the value of the next least significant bit.

A fourth C/4 or LSB capacitor is required to make the total capacitive array have a value of 2C.

Switched Capacitor SA ADC



The switches S1 - S4 are MOSFETs that are turned off or on as dictated by the flip flops in the successive approximations register (SAR).

The inputs are the analog signal to be digitized V_{in} and the DC reference voltage V_{ref}. The comparator output goes to control the successive approximations register logic.

The ADC outputs are from the SAR flip flops.

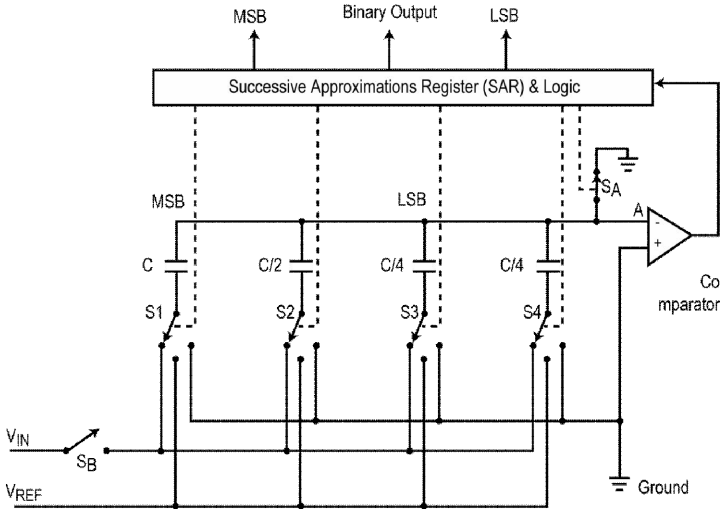
Capacitive SA ADC Operation

Before conversion, SA is closed connecting the common capacitor bus A and the comparator input to ground. S1 through S4 are connected to the input voltage line. Switch SB is closed. The output of the comparator is zero.

During this time, all capacitors are in parallel and the total capacitance is 2C. The capacitors charge up to the input analog input voltage.

All capacitors have the same total charge Q_T.

When the conversion is started, switch SB is opened. This stores the input signal sample on the capacitor array. This is the sampling of the input.



Capacitive SA ADC Operation

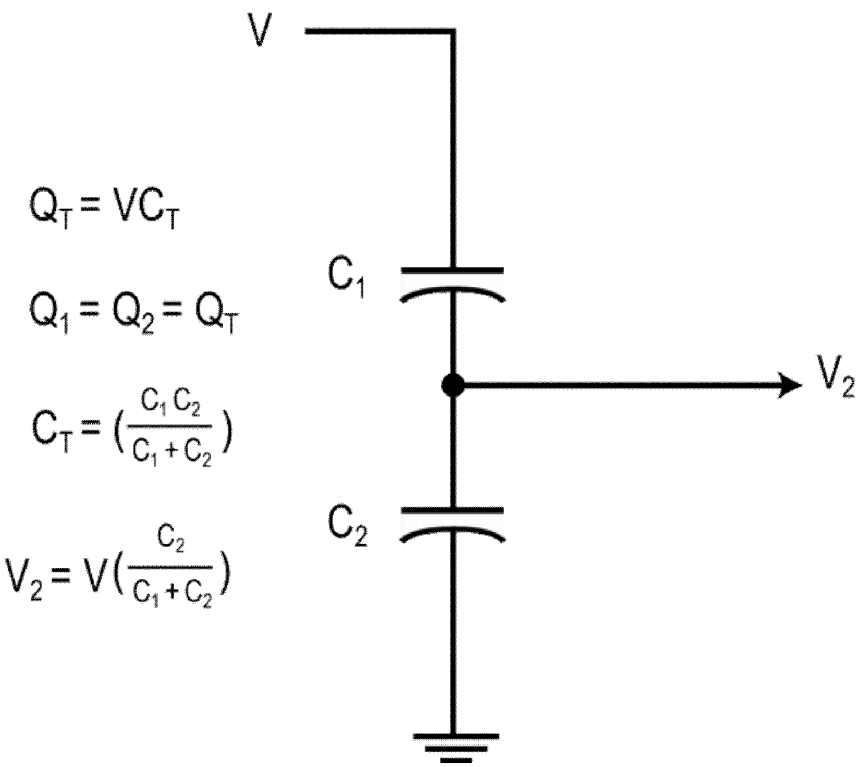
The successive approximations algorithm switches S1, S2, and S3 between the reference voltage and ground one at a time from the MSB to the LSB to bring the comparator input as close to zero as possible.

During this process, the capacitors actually form a voltage divider whose output goes to the comparator input.

The idea is to balance the charge on the capacitors until a near zero input is achieved. When this condition occurs, conversion is complete and the binary state of the flip flops controlling the switches on the capacitors is the digital output. This is the quantization part of the conversion.

Switched capacitor ADCs are often called charge redistribution converters.

Capacitive Dividers



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Capacitor Review

When a capacitor C is charged by a voltage V, a charge in coulombs Q on the capacitor is Q = CV.

When capacitors are connected in series to form a voltage divider, their total capacitance is

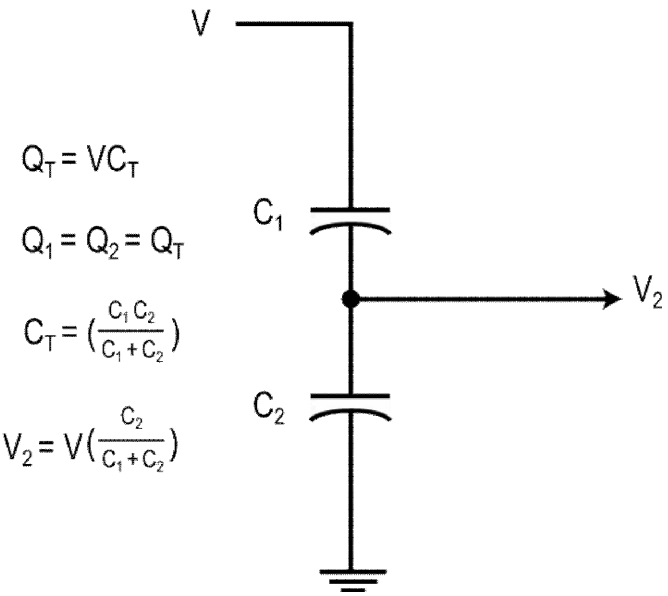
$$C_T = C_1C_2/(C_1 + C_2)$$

The charge on each capacitor is equal to the total charge Q_T.

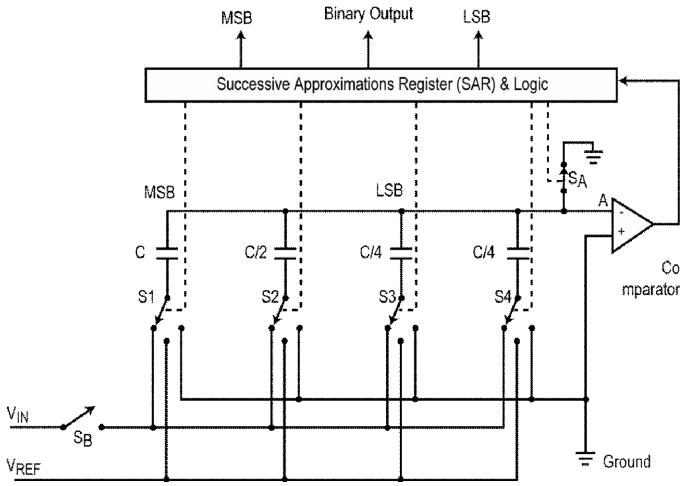
$$Q_T = Q_1 = Q_2$$

The voltage at the output of the divider across C_2 is:

$$V_2 = V(C_1/C_1 + C_2)$$



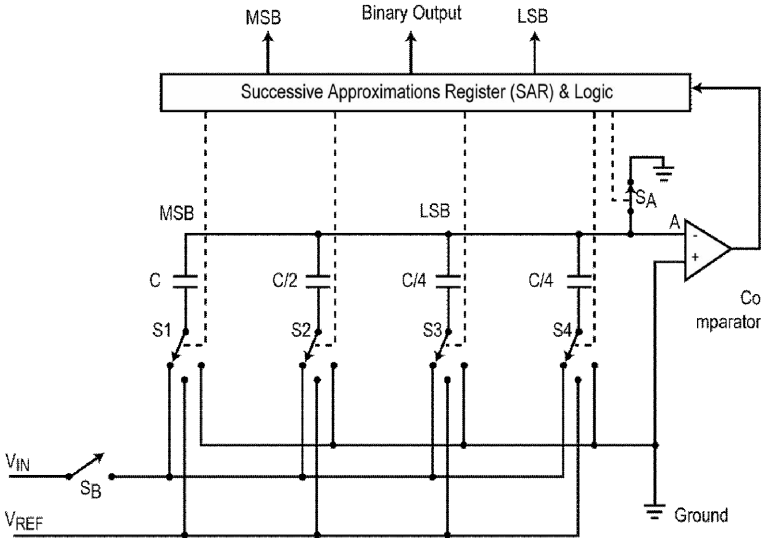
Capacitive SA ADC Circuit Operation



When the start conversion signal is received, switches SA and SB open. The bottom terminals of the capacitors are switched to ground. The analog voltage sample is trapped and stored in the capacitor array like the capacitor in a S/H amplifier.

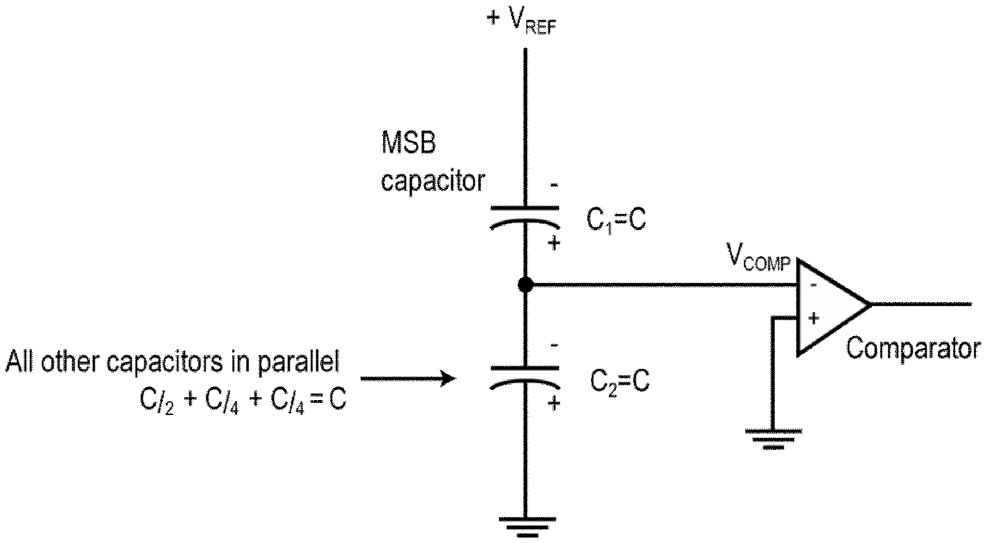
With the capacitors' lower terminals at ground, the input to the comparator is $-V_{in}$ because the switching reverses the capacitor connection to the comparator. If the input is a positive voltage, the voltage at point A will be negative.

Capacitive SA ADC Circuit Operation



The lower end of the MSB capacitor is first switched from ground to V_{ref}. All the remaining lower capacitor plates remain connected to ground. This produces a capacitive voltage divider with the C capacitor on top and all the other capacitors connected in parallel to also equal C.

Circuit Operation



$$V_{COMP} = V_{REF}\left(\frac{C_1}{C_1 + C_2}\right)$$

$$= V_{REF}\left(\frac{C}{2C}\right) \quad = V_{REF}/_2$$

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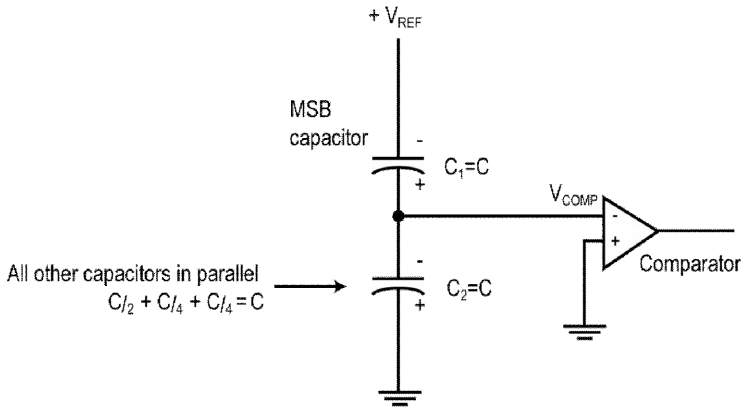
Capacitive SA ADC Circuit Operation



$$V_{COMP} = V_{REF}\left(\frac{C_1}{C_1 + C_2}\right)$$

$$= V_{REF}\left(\frac{C}{2C}\right) = V_{REF}/_2$$

The comparator input is forced in a positive direction by an amount equal to one half the reference voltage value ($V_{ref}/2$).

If the input is greater than $V_{ref}/2$, then the comparator input will be ($-V_{in} + V_{ref}/2$) which will be a negative value. When this value is compared to ground in the comparator, the comparator output is a binary 1 indicating the MSB is greater than the input value. Therefore, the comparator tells the SAR logic to keep the MSB set.

Capacitive SA ADC Operation

If V_{in} is initially less than $V_{ref}/2$, the comparator output is a binary 0 so the MSB flip flop is reset.

The SAR logic next sets the most significant bit and the process continues until all bits have been tested.

Most modern capacitor array SA ADCs have built in calibration circuitry that helps to offset any errors that develop as the result of inaccurate capacitor values. MOSFET switches automatically turn off or on to connect or disconnect small values of capacitors (< the LSB C value) to make sure that the capacitor values are accurately binary weighted. Such ADCs contain a calibration mode that is activated during power up to ensure full accuracy, linearity, and monotonicity.

Capacitive vs. R-2R SA ADCs

Capacitive ADCs take up much less space on chip than a resistor network ADC.

Capacitive ADCs can be made with standard low cost digital CMOS and are easily integrated into microprocessors or other system level chips.

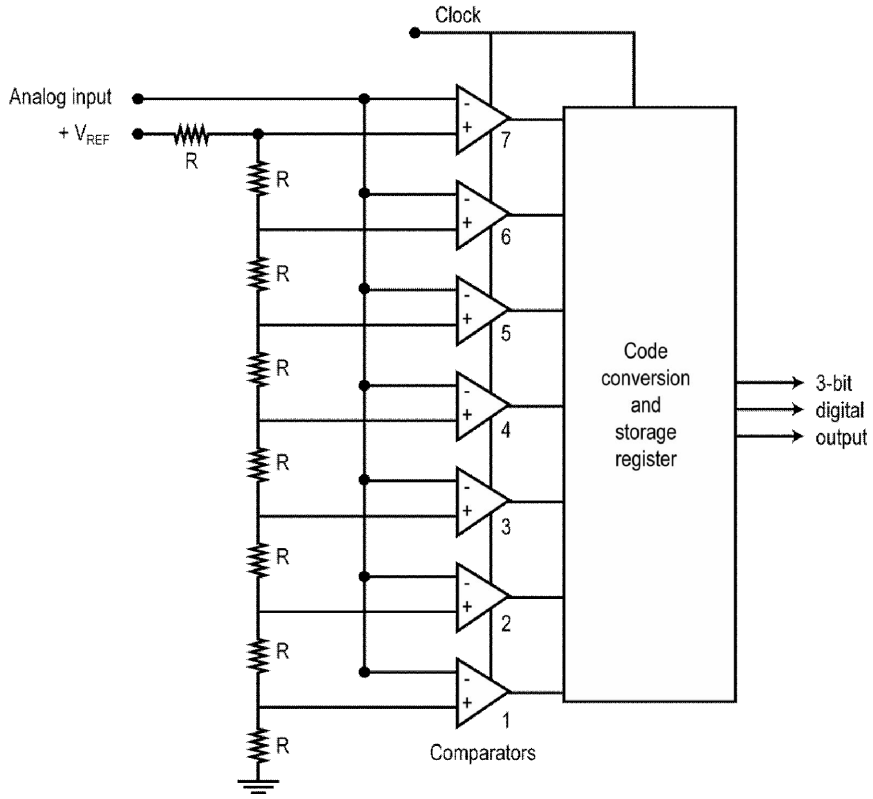
Capacitive ADCs store the input sample so no separate S/H amplifier is needed.

Capacitive ADCs are faster than R-2R ADCs.

Capacitive ADCs have automatic calibration circuits that ensure linearity and accuracy.

Capacitive ADCs can have as many as 16-bits with speeds up to about 5 mega samples per second (MSPS) conversion time.

Flash Converters



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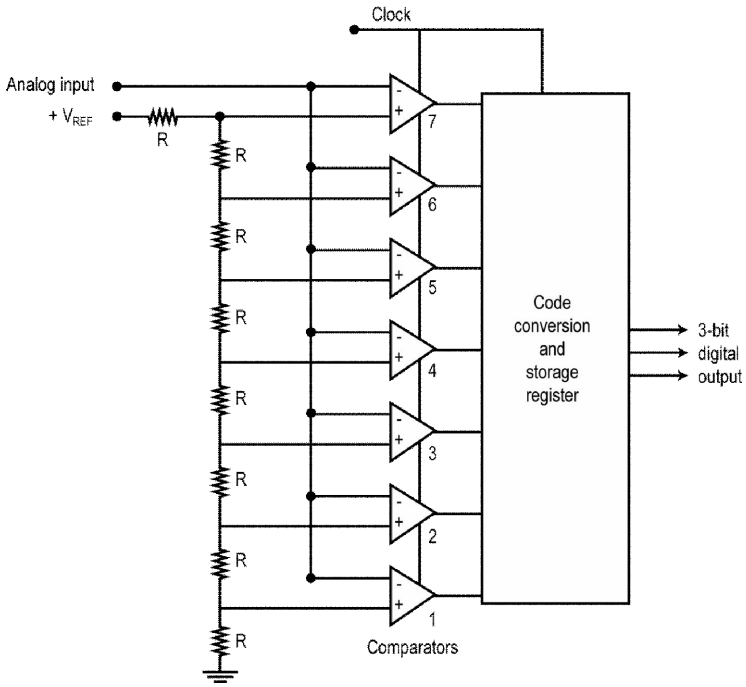
Flash Converters

A flash converter is the fastest type of analog-to-digital converter (ADC). It is also known as a simultaneous or parallel converter.

The simplified 3-bit flash converter shown here illustrates the concepts. With 3-bits, it can resolve $2^3 = 8$ discrete voltage levels.

The reference voltage is applied to a voltage divider that divides the reference into eight voltage levels. These levels are applied to inputs to the seven comparators.

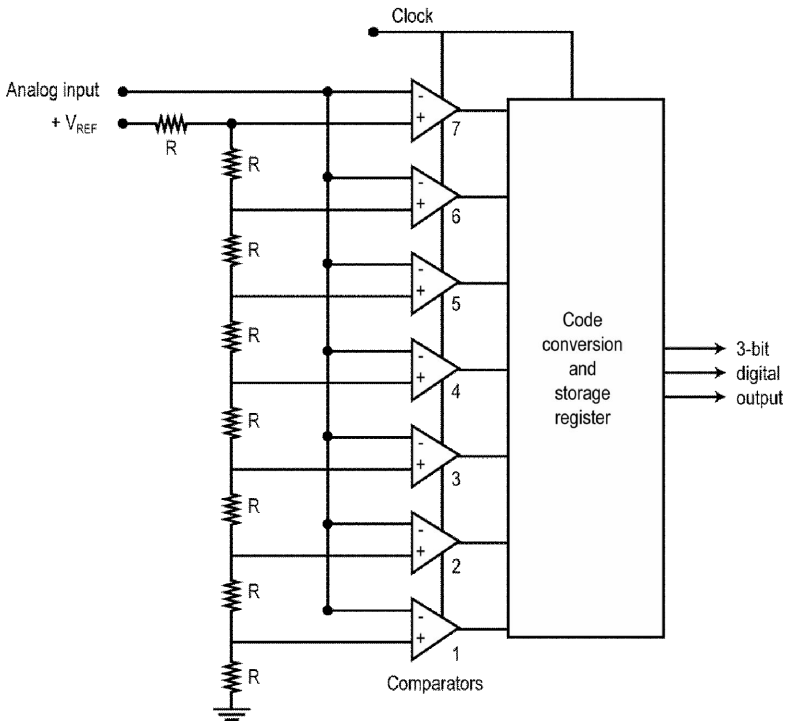


Flash Converters

The analog input to be digitized is applied to all of the comparator's other inputs.

The comparators compare the input level to the seven voltage levels simultaneously.

The comparators produce a binary 0 or binary 1 output depending upon whether the input voltage is greater than or less than the voltage level from the voltage divider.



Flash Converter Operation

The analog input is simultaneously compared to all of the voltage levels from the divider simultaneously. If the input is greater than the voltage level from the divider, the comparator output is binary 1.

If the reference voltage is 10 volts, the voltage divider divides the 10 volts into eight levels. There are eight voltage levels from zero to 8.75 volts in 10/8 = 1.25 volt increments.

With zero input, all comparator outputs are zero. As the analog input increases, the comparator outputs become binary 1 as the voltage exceeds the value from the divider. The comparator outputs become binary 1 from bottom to top as the voltage increases. The output from the comparators is called a thermometer code since the binary 1 bits "rise" as the input voltage increases.

A code conversion circuit translates the thermometer code to the standard 3-bit binary equivalent code and stores it in a register.

Facts About Flash Converters

Because the analog input is compared simultaneously to all increments for voltage from the divider at the same time, the output code appears very fast. Speed of conversion is limited only by the speed of the comparators and the propagation delay for the binary code conversion logic.

Conversion speeds are in the nanosecond region. Sampling rates can be as high as 5 GSPS (giga samples per second) for off-the-shelf ADC chips. Rates of up to 20 GSPS have been achieved in proprietary chip designs.

The resolution is limited by how many comparators can be made on a chip. Flash converters require $2^N - 1$ comparators where N is the desired number of bits. To make an 8-bit ADC, $2^8 - 1 = 255$ comparators are needed.

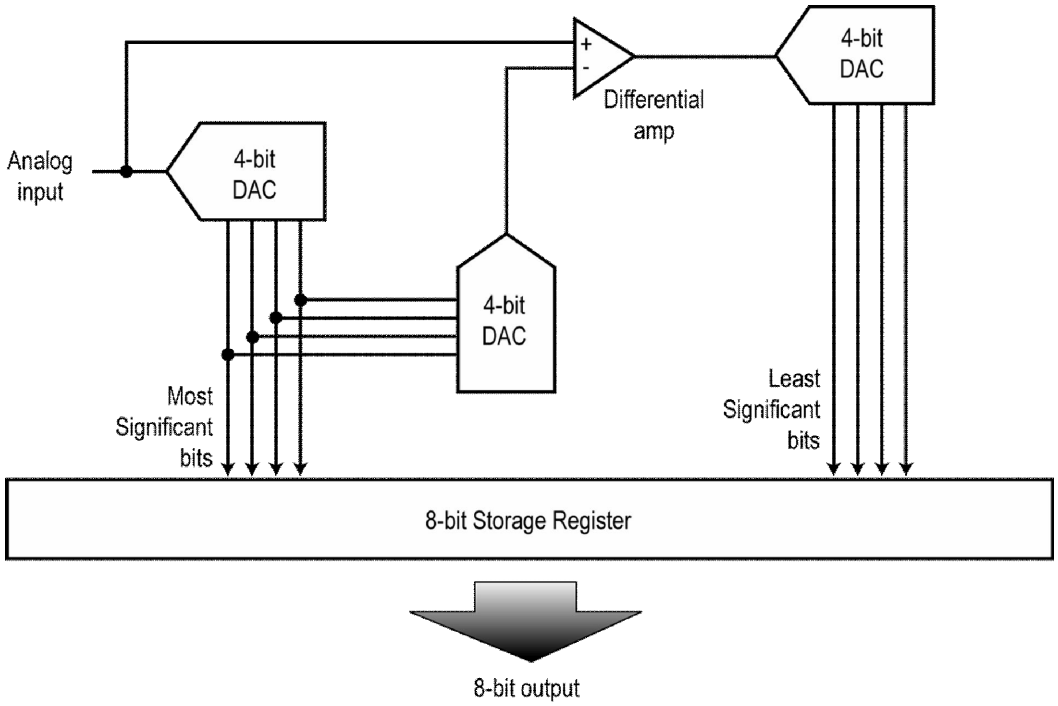
Facts About Flash Converters

Comparators are linear circuits that require lots of chip space and have a large power consumption. Flash converters have the highest power consumption of any ADC. This is a major disadvantage but it's the price you have to pay for the speed.

The number of comparators doubles for each additional bit of resolution. A 9-bit ADC requires 511 comparators, a 10-bit comparator requires 1023 comparators. This is the extreme upper limit for practical chips. Most practical flash converters are 8-bits or less.

Flash converters make it possible to digitize video signals as well as radio frequency signals bringing digital processing to these applications.

Pipeline Converter Operation



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Pipeline Converters

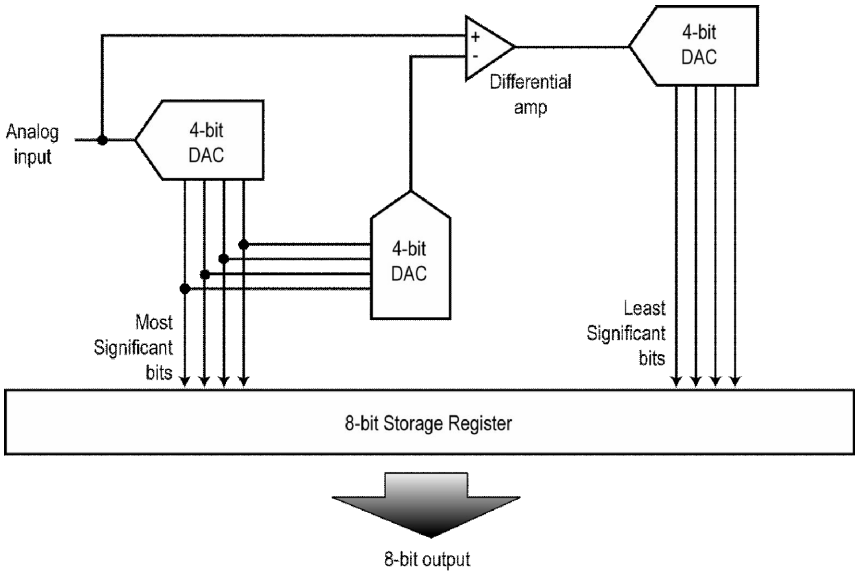
Pipeline converters use flash converters to produce high sampling rates but use several stages of conversion to reduce the total number of comparators needed.

Pipeline converters are also called subranging converters.

The total number of comparators is greatly reduced for a desired resolution but the total conversion time is increased.

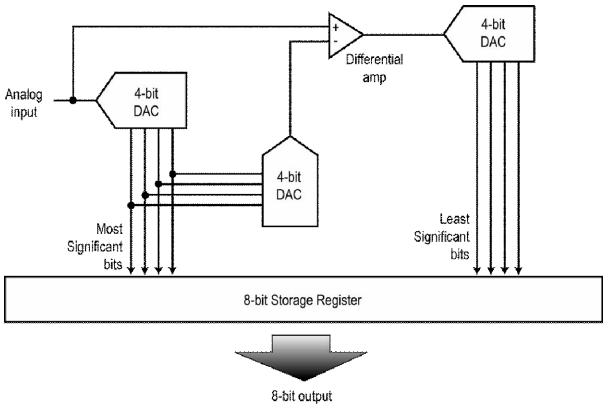
While pipeline converters are slower than flash converters, they are still much faster than successive approximation converters so find wide application.

Pipeline Converter Operation



The 8-bit converter simplified pipeline converter shown here uses two 4-bit flash converters to achieve the desired resolution. Instead of the 255 comparators dictated by a flash design, the pipeline converter uses two 4-bit flash converters each with 15 comparators for a total of 30. This is called a half flash converter.

Pipeline Converter Operation



The input is first sampled in a S/H amplifier (not shown) to eliminate aperture error. The sampled voltage level is applied to the first 4-bit flash ADC. Its four output bits become the four most significant bits of the output.

The four output bits from the first flash converter are also applied to a 4-bit DAC that converts the data back to analog. This analog value is subtracted from the original analog input in a differential amplifier.

The differential amp output represents the remaining one sixteenth of the input is then converted by another 4-bit flash ADC to produce the four least significant bits of the output.

Facts About Pipeline Converters

The pipeline or subranging concept can be extended by using three, four, or more flash conversion steps to achieve higher resolution while minimizing the number of comparators, the chip size, cost, and power consumption. 12 and 14-bit pipeline converters are available.

A half flash converter can often achieve conversion speeds of up to 100 MSPS with a resolution of 8-bits. This is less than a pure flash but much faster than available successive approximations ADCs.

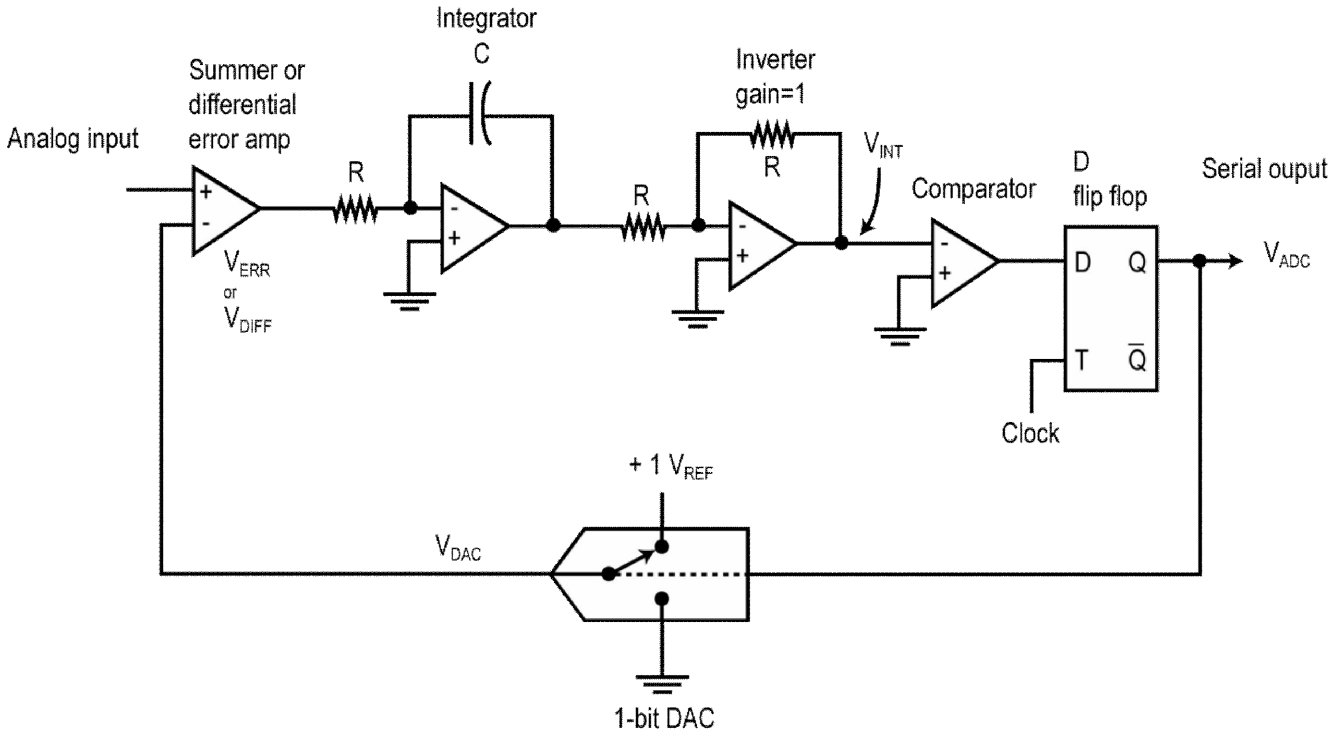
Sigma-Delta Converters

A sigma-delta ($\sum$ - Δ) converter is a special form of ADC that uses the concept of oversampling to reduce noise and increase resolution in the conversion process.

Sigma-delta converters are used primarily in audio applications but also find application in low frequency or DC industrial measurements of signals from sensors.

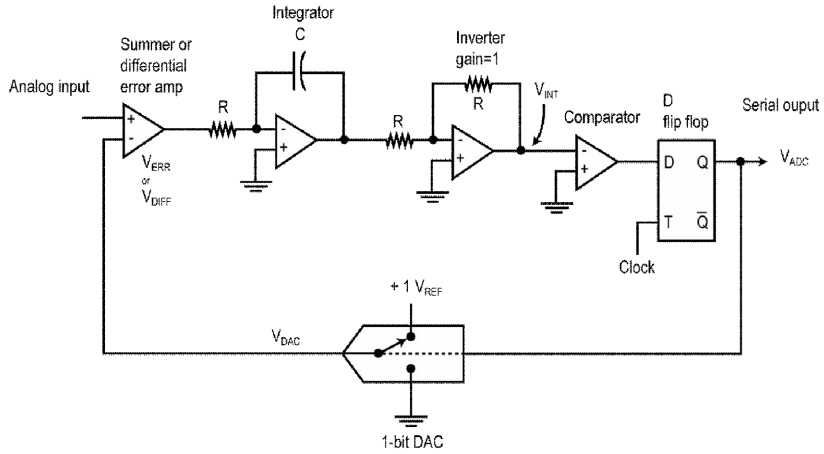
Sigma-delta converters feature wide dynamic range, high signal to noise ratio, and very high precision or resolution typically 16- to 24 bits. This is more than any other type of ADC.

Sigma-Delta Converters



A discussion of this graphic is presented in the pages that follow. You can print this graphic for study purposes before going on.

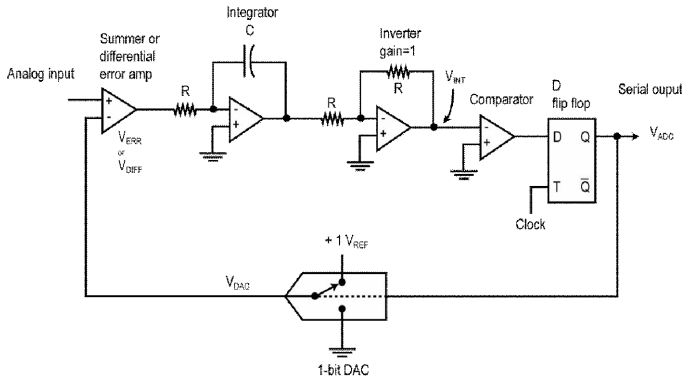
Sigma-Delta Converters



The heart of a simple ∑ - Δ converter is called the ∑ - Δ modulator. The analog input signal V_{in} is applied to a differential amplifier summing circuit along with the output from a one bit DAC. The circuit output is usually called the error signal V_{err} or the difference voltage V_{diff}.

The summing circuit output is applied to an integrator. The integrator is typically an op amp inverter with a capacitor in the feedback path with a long time constant compared to the clock frequency.

Sigma-Delta Converters



The time constant (RC) is set so that, in effect, the integrator simply adds the present error signal to the voltage previously stored on the capacitor to generate the next integrator output voltage state.

The integrator output is inverted by an op amp inverter producing a signal V_{int} that is applied to a comparator.

The comparator output is either +5 volts (binary 1) or zero volts (binary 0). The way to view the comparator is a one bit ADC where the output is either 0 or 1 depending upon if the input is less than or more than zero volts.

∑ - Δ Operation

The comparator (ADC) output is latched into a D-type flip flop (FF) by an input clock signal. The clock determines the oversampling rate. On each clock pulse, the input state is sampled, stored in the integrator, and used to update the comparator output.

The FF output is also applied to the DAC. A one bit DAC has an input that is 0 or 1 and whose output is either of two voltage references. Examples are +1 V and -1 V or +1 volt and 0 V. For this circuit, assume 0 V (ground) and +1 volt.

The output from the comparator and thus the FF is a serial binary signal whose DC average is equal to the analog input signal.

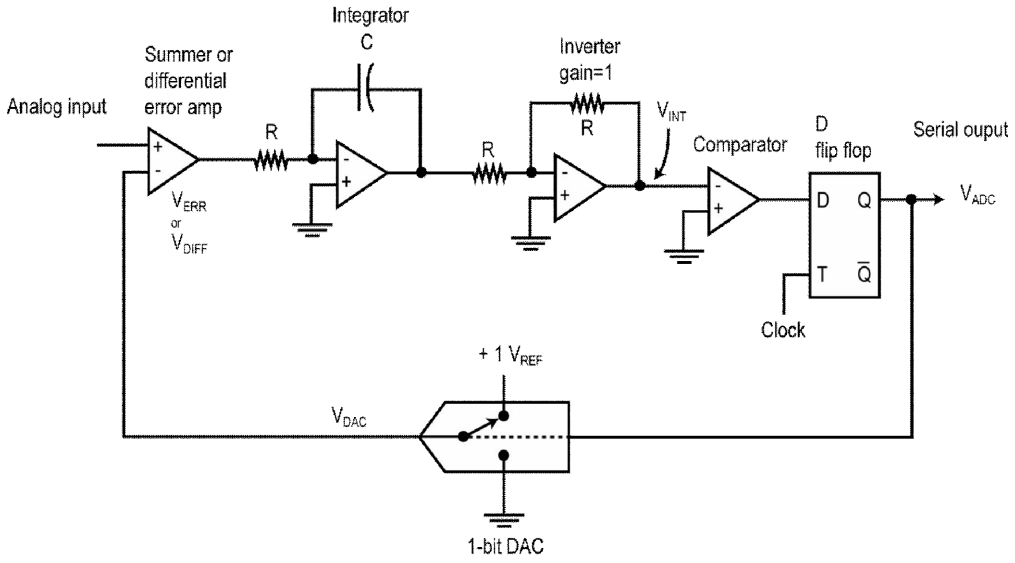
∑ - Δ Operation

A high speed clock signal controls the operation of the circuit by causing the circuit to repeatedly sample the input signal level and to update the integrator, make the comparison, and either set or reset the FF.

The sampling rate is much higher than the Nyquist rate requirement on all other ADCs. The sampling rate is typically 4 to 128 times the highest frequency content of the input signal. This is called oversampling. A typical oversampling factor is 64 times the maximum input signal frequency. For an audio upper signal level of 20 kHz, the sampling clock might be 64 x 20 kHz = 1280 kHz or 1.28 MHz.

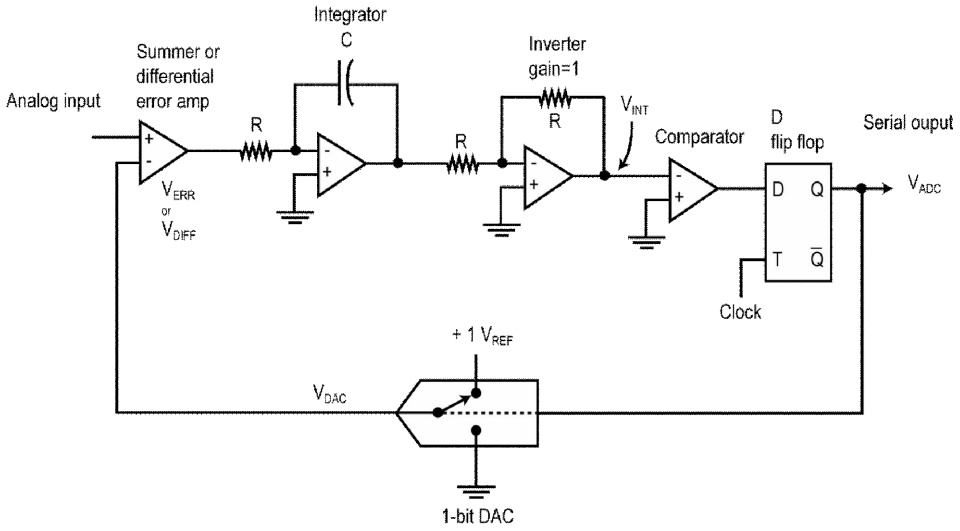
Oversampling has the effect of shifting the quantization noise to a frequency range well beyond the input bandwidth. This noise is easily filtered out thereby giving the ∑ - Δ converter a higher signal-to-noise ratio than traditional converters.

Time Domain Operation of the ∑ - Δ Modulator



Assume a fixed analog input voltage of 0.7 volts. The DAC output is either 0 or +1 volt depending upon the binary input. Assume that the comparator output is initially zero so the FF is reset and the DAC output is zero. The error voltage V_{diff} is +0.7 V. The integrator output becomes -0.7 V but the inverter changes this back to +0.7 V. In this analysis, V_{int} is the inverted integrator output from the inverter.

Time Domain Operation of the ∑ - Δ Modulator



On the next clock pulse, the integrator output is compared to ground so the comparator output switches high. The clock sets the FF so the DAC output then goes to +1 V. The error voltage V_{diff} goes to -0.3 volts. The integrator output from the inverter V_{int} then goes 0.7 – 0.3 = 0.4 volts.

The comparator output stays at binary 1 so the FF remains set and the DAC output remains 1. The error voltage is still 0.3 but that is added to the previous integrator state to produce 0.1 volt. This process continues producing the results shown in the Table 1.

Table 1

V_{IN}	$V_{DIFF(n)}$	$V_{INT(n)}$	$V_{INT(n-1)}$	$V_{ADC(n)}$	$V_{DAC(n)}$
0.70			0.00	0.00	0.00
0.70	0.70	0.70	0.00	1.00	1.00
0.70	-0.30	0.40	0.70	1.00	1.00
0.70	-0.30	0.10	0.40	1.00	1.00
0.70	-0.30	-0.20	0.10	0.00	0.00
0.70	0.70	0.50	-0.20	1.00	1.00
0.70	-0.30	0.20	0.50	1.00	1.00
0.70	-0.30	-0.10	0.20	0.00	0.00
0.70	0.70	0.60	-0.10	1.00	1.00
0.70	-0.30	0.30	0.60	1.00	1.00
0.70	-0.30	0.00	0.30	1.00	1.00
0.70	-0.30	-0.30	0.00	0.00	0.00
0.70	0.70	0.40	-0.30	1.00	1.00
0.70	-0.30	0.10	0.40	1.00	1.00
0.70	-0.30	-0.20	0.10	0.00	0.00
0.70	0.70	0.50	-0.20	1.00	1.00
0.70	-0.30	0.20	0.50	1.00	1.00
0.70	-0.30	-0.10	0.20	0.00	0.00
0.70	0.70	0.60	-0.10	1.00	1.00

Repeating sequence

Source: “Delta-Sigma Converters Simplified”, ECN Magazine, November 15th, 2003

Table 1 Legend

V_{in} = analog input voltage to be digitized

V_{diff} = differential amplifier output error voltage

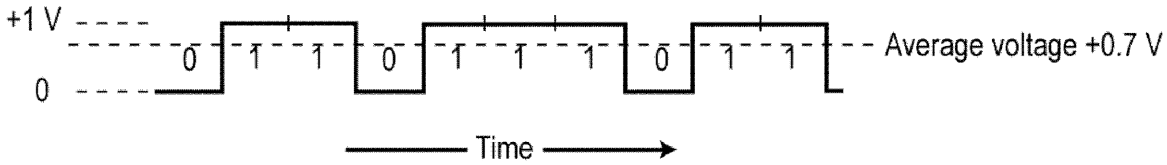
$V_{int}(n)$ = output of the integrator inverted at clock time n

$V_{int}(n - 1)$ = output of the integrator inverted at the previous clock time n – 1

V_{adc} = output of the modulator FF

V_{dac} = output of the 1-bit DAC

Time Domain Operation of the ∑ - Δ Converter

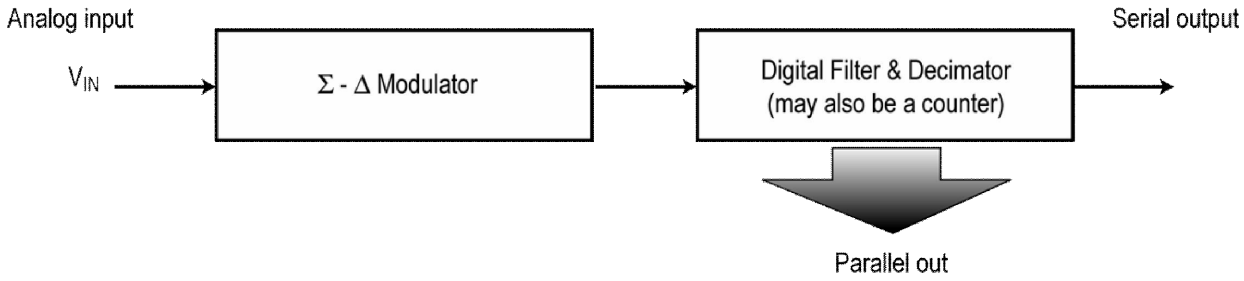


The term n is the current clock time while n – 1 is the previous clock time.

If the input voltage remains constant, the serial binary output will have a repeating pattern of 0110111011 (from top to bottom in the table). If the FF output is either 0 or +1 volt then with 7 of the 10 bits being +1 volt and 3 bits of 0 V the average output from a low pass filter will be 7/10 = 0.7 volts.

If the input signal is changing as is the more usual case, the average number of binary 1 bits will increase with an increasing input voltage and decrease with a decreasing voltage.

∑ - Δ Converter



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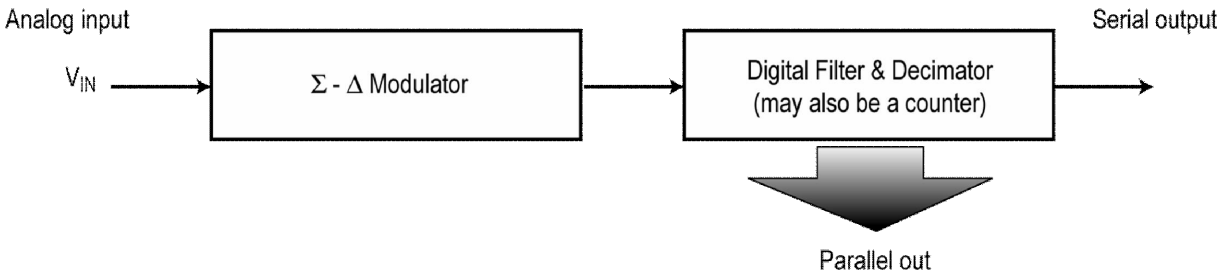
∑ - Δ Converter

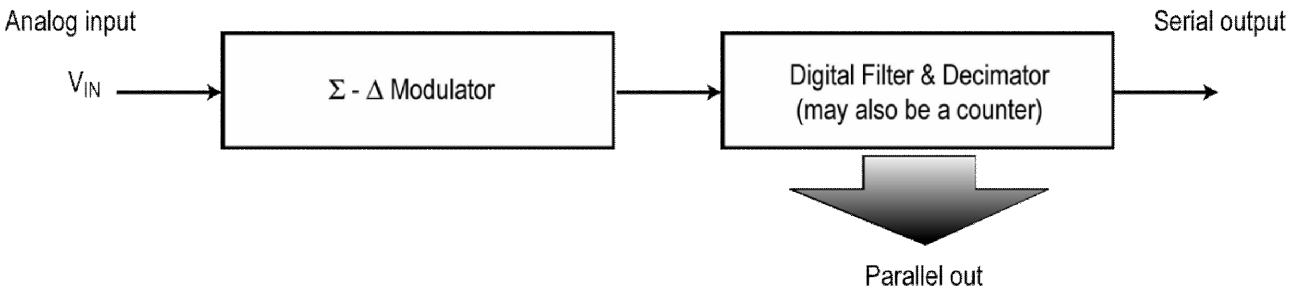


The serial binary signal from the ∑ - Δ modulator is passed through a digital low pass filter and a decimator circuit that converts the high speed serial signal to a lower speed signal made up of a sequence of fixed length binary words.

One way to visualize this process is to assume that the serial output of the modulator is fed to a binary counter that counts the number of binary 1 bits and, after a certain interval, produces a fixed length (such as 16-bits) binary output word.

The digital filter and decimator are DSP circuits and beyond the scope of this module.

∑ - Δ Converter



The output of the ∑ - Δ converter may be serial or parallel binary bits. Typical word sizes are 16, 18, 20, 22 and 24 bits.

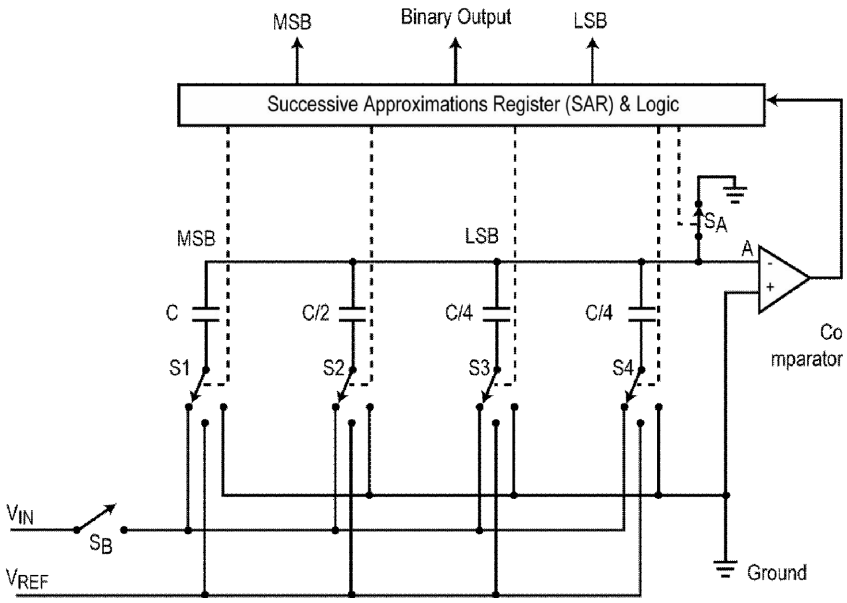
Most ∑ - Δ converters are integrated circuits and many use two or more cascaded internal ∑ - Δ modulators to improve upon the SNR.

The process of oversampling shifts the quantization noise to a frequency well beyond the input signal frequency making it easy to filter out. The result is that the sigma-delta converter has the best signal to noise ratio of any ADC.

Comparison of ADC Types

Type of ADC	Sample Rate (maximum)	Resolution (maximum)	Application	Advantage or disadvantage
Successive Approximation	2 to 5 MSPS	16-bits	General purpose	Simplest, least expensive
Flash	1 to 2 GSPS	8-bits	Video, RF	Most expensive, power hog
Pipeline	5 to 125 MSPS	12 to 14 bits	Video, software radios	Best compromise, all factors
Sigma-delta	Maximum bandwidth – 1 MHz	16 to 24 bits	Audio, sensor data	Best resolution and SNR

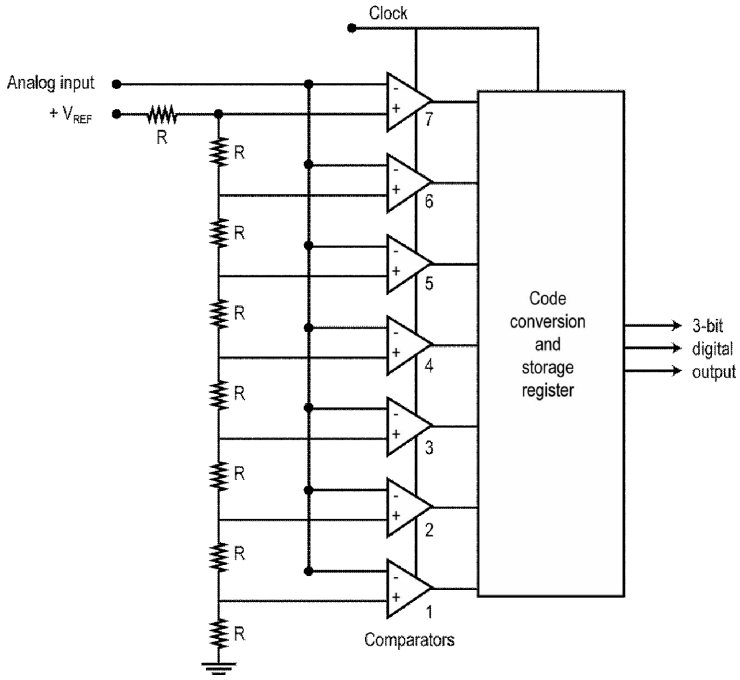
ADC Comparisons: SA



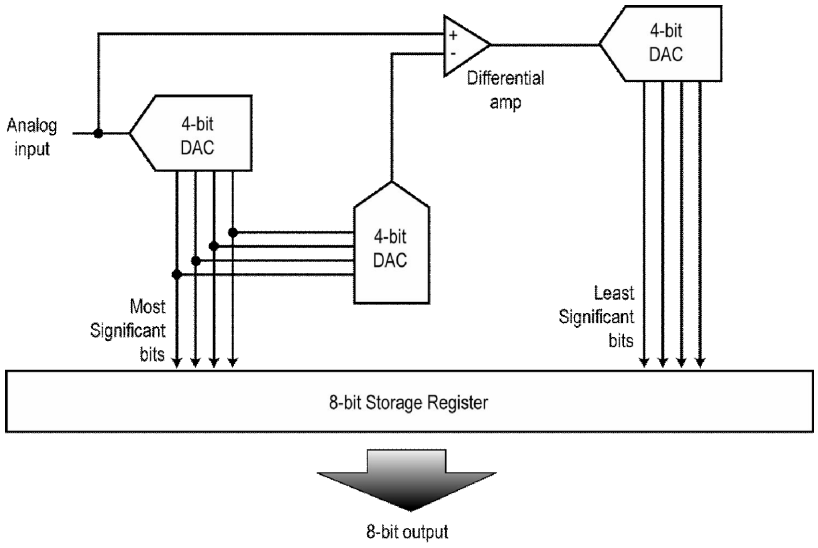
The successive approximations converter is the oldest and most widely used. It is also the least expensive and has the lowest power consumption. Its maximum resolution is 16-bits because of the difficulty of making R-2R or capacitive dividers accurate enough. The upper sample rate is 2 to 5 MSPS.

ADC Comparisons: Flash

The flash converter is by far the fastest. Resolution is limited by the number of comparators practical in an IC. 8-bit resolution is the highest practical. Sample rates to up to 2 GSPS make the flash ADC ideal for converting video or even radio frequency (RF) signals. This ADC is very expensive and consumes enormous power.

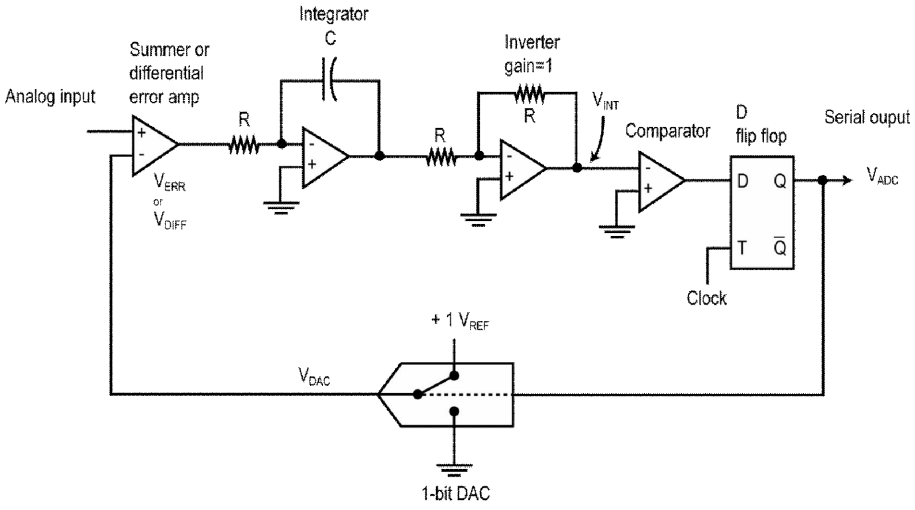


ADC Comparisons: Pipeline



The pipeline ADC uses small flash converters in a pipeline to achieve higher resolutions at the expense of speed. But sample rates up to about 125 MSPS with 10, 12 and 14-bit resolution are practical with reasonable cost and power consumption. It is the best current compromise design.

ADC Comparisons: ∑ - Δ



The sigma-delta converter is a special case since it uses oversampling. The typical upper frequency limit of the input is about 1 MHz. Most applications like audio and industrial sensor digitization use far less bandwidth. The ∑ - Δ ADC also has the highest resolution and best (highest) signal to noise ratio with reasonable power consumption.

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Types of Analog-to-Digital Converters

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