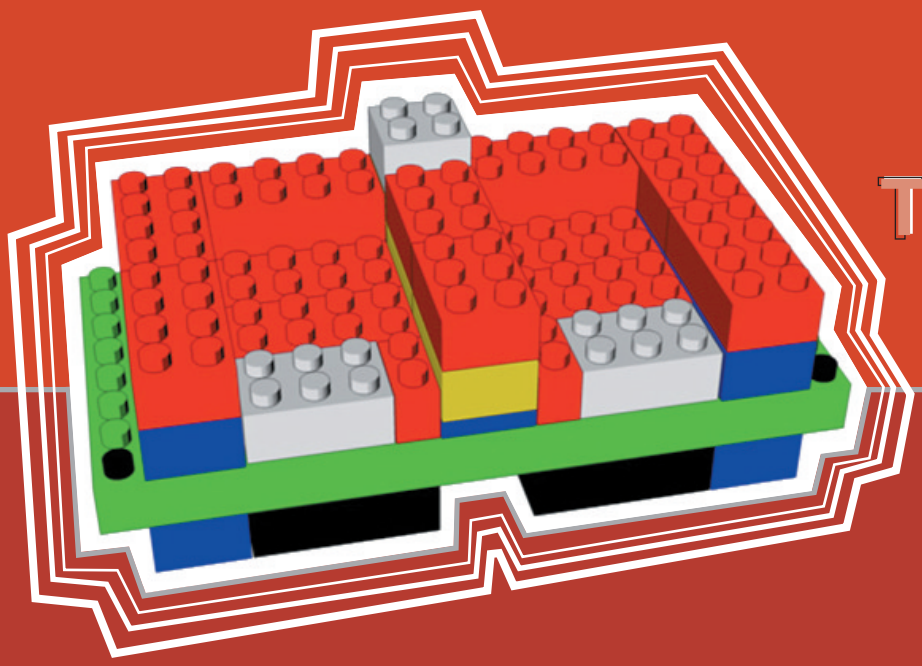


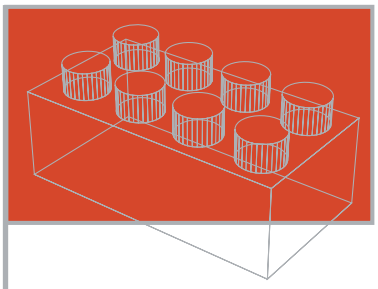
TRANSISTOR MODEL Assembly KIT

PARTICIPANT WORKBOOK

A simulation activity for use in developing interest and skills in semiconductor manufacturing fundamentals. Created in partnership with Advanced Micro Devices.

Transistor Model Assembly Kit

First Edition, 2001



To order these materials or for more information, contact:

Maricopa Advanced Technology Education Center (MATEC)
2323 West 14th Street, Suite 540
Tempe, Arizona 85281-6950
Phone (480) 517-8650
FAX (480) 517-8669
E-mail: matec@domail.maricopa.edu
Web Site: http://www.matec.org

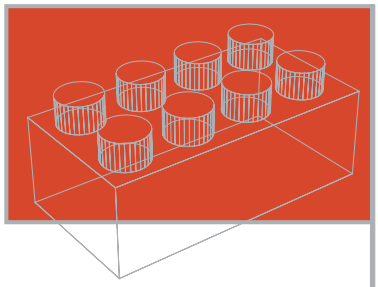
Support for this work was provided in part by the National Science Foundation's Advanced Technology Education (ATE) Program through grants #DUE 9602373 and 990849.

Any opinions, findings, and conclusions or recommendations expressed in the material are those of the authors and do not necessarily reflect the views of the National Science Foundation.

National Science Foundation

Acknowledgements

"A building-blocks approach to learning how a basic transistor is manufactured."



The transistor model kit is designed to simulate the manufacturing processes and materials used in the construction of a basic transistor. The model assembly activity can be performed individually by a student or by students working in a teams of two to six. The recommended group size is four.

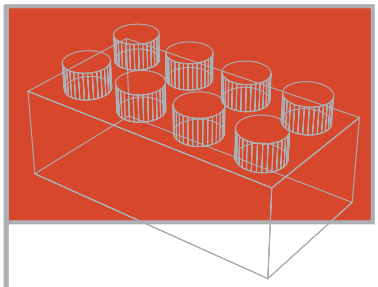
This transistor model kit and the training activity that evolved from the model were created by Julian Serda and Cynthia Wyman, technical instructors, Advanced Micro Devices, Austin, Texas, in 1998. This transistor model assembly activity has been successfully implemented in AMD's new-employee orientation program, AMD's Summer Institute for Educators, and has been shared with Austin-based semiconductor companies for use in their own teacher workshops.

The color-rendered graphics of the transistor model were created by John Olson, MATEC.

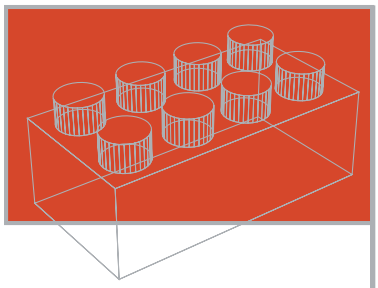
The Participant Workbook layout was designed by Bryan McIntyre, MATEC.

The Participant Workbook was written by Tito Laurel, Industrial Electronics and Math teacher at Travis High School, and edited by Julian Serda, Senior Learning and Development Specialist, AMD.

Table of Contents



Preface



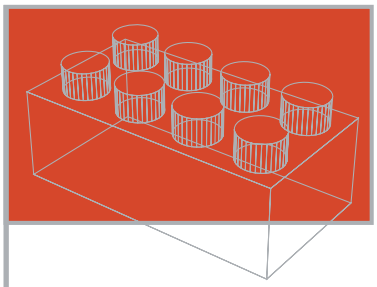
Learning how a transistor is manufactured is to truly appreciate man's ingenuity. The challenge presented before industry is how to construct devices at the molecular level, having them function at competitive standards, while operating for long periods of time. Inherent in the manufacturing process is the layering of chemical composition and thickness, then cutting away specified sections before starting the whole process again.

This would be similar to building a house the following way:

1. Lay a concrete slab.
2. Add a 10-foot layer of solid brick on the slab.
3. Mark where you want the inside room to be.
4. Cut away the center of this solid brick, leaving an outside wall around 10 inches thick.

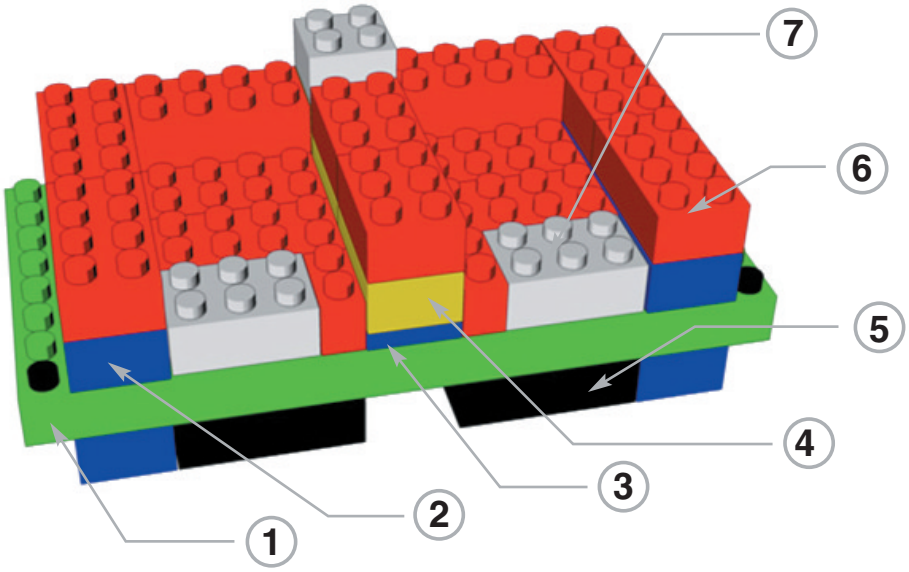
One thing missing would be to add insulated wires and outlets to get electricity into the house. The trick is to figure out how to do this when you're restricted to adding only whole layers at a time. The other tool you have is that you can cut away any part you don't want before adding another layer. In adding wiring to a house would you start by adding a layer of metal first, then cutting away the part you don't need, then adding insulation on top of it? Or would you start by adding insulation material first? How to understand this layering process is the focus of this work—done in the simplicity of plastic building blocks. Familiarize yourself with the process involved as well as the explanations. Look for the patterns in the process of adding the same kinds of materials; look at why those specific materials of specified chemical makeup were chosen, then focus on how each step contributes toward the final model.

Transistor Model Assembly Performance Objective



Given a complete Transistor Model kit, each participant (individually or in a team of two to six) will be able to model the fabrication process of a basic transistor. The completed model will match the picture shown on the cover of the participant workbook.

Transistor Model

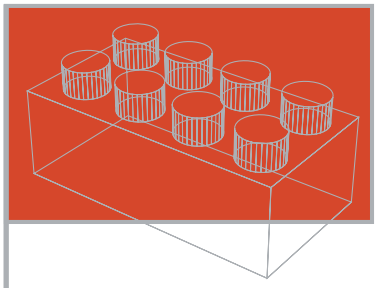


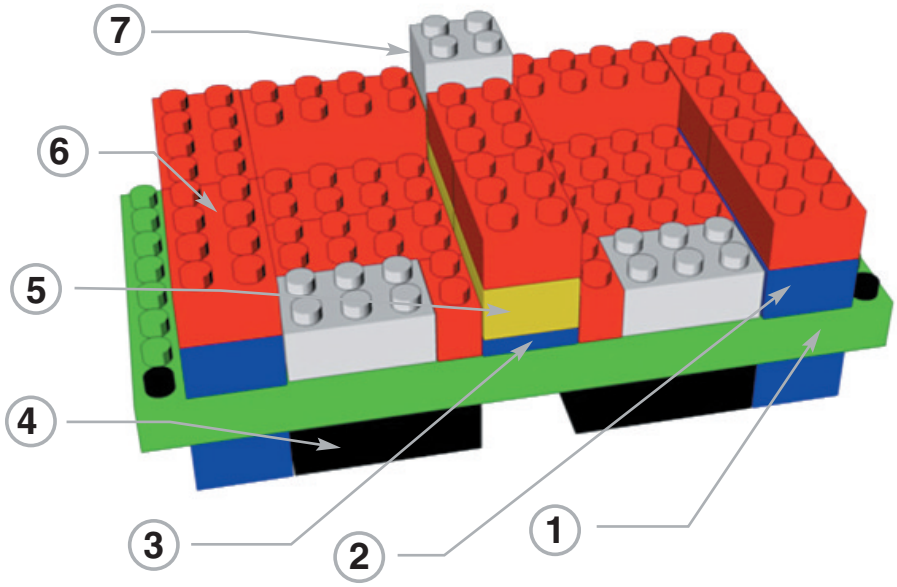
1	Substrate
2	Field Oxide+
3	Gate Oxide
4	Polysilicon Gate
5	Source & Drains
6	Top Nitride
7	Metal Contacts

The transistor you are going to construct is shown above. The differently colored blocks represent various features of a basic transistor. The numbers indicate the major parts of the transistor and the order in which they are produced.

1. **Substrate** — Made of silicon serving as the foundation for building the transistor.
2. **Field Oxide** — Barrier of silicon dioxide isolating the transistor from other components of a larger integrated circuit.
3. **Gate Oxide** — Thinnest oxide film electrically isolating the gate of the transistor from the substrate.
4. **Polysilicon gate** — Narrowest feature of a transistor serving as the input of the transistor.
5. **Source and Drain regions** — Areas forming active (conductive) regions for the transistor's output.
6. **Top Nitride** — Thick film protecting the transistor from the environment.
7. **Metal Contacts** — Electrodes allowing electrical connections to the gate, source, and drain of the transistor.

Transistor Model





Question #1 / Matching

Match the numbered part with the corresponding lettered answer.

_____ **A. Gate Oxide** — Thin oxide film of the gate structure.

_____ **B. Top Nitride** — Thick, protectant film for the transistor.

_____ **C. Substrate** — Silicon-based foundation of the transistor.

_____ **D. Metal Contacts** — Three electrodes allowing electrical connections of the transistor.

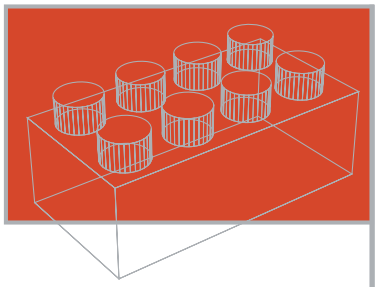
_____ **E. Source and Drain Regions** — Conductive regions for the transistor's output.

_____ **F. Field Oxide** — Silicon dioxide barrier that isolates the whole transistor.

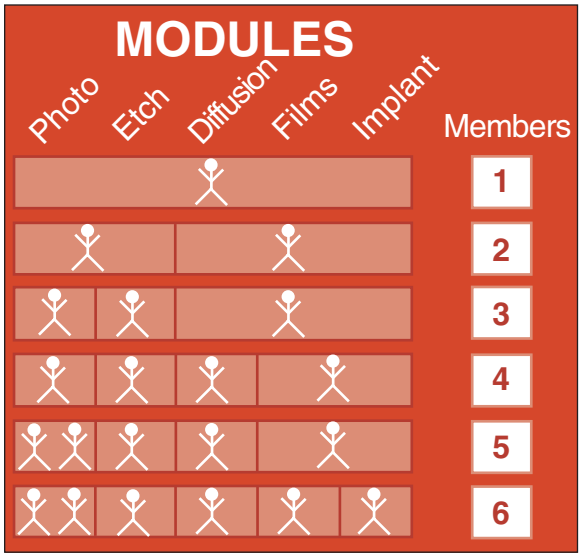
_____ **G. Polysilicon gate** — Material of which the gate structure is made.

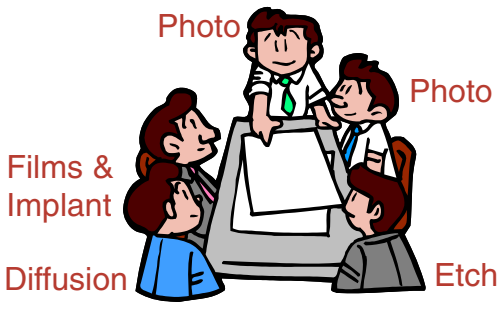
Answers: A-3, B-6, C-1, D-7, E-4, F-2, G-5

Table Layout



Given the number of members in your group, make the following module assignments.





One person in group
- * You do it all

Two participants in group
- * Photo, Etch
- * Diffusion, Films, Implant

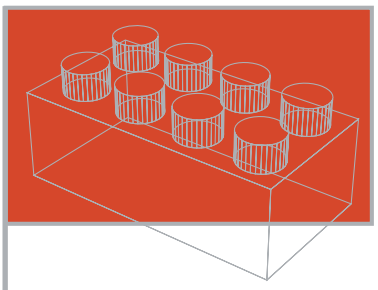
Three participants in group
- * Photo
- * Etch
- * Diffusion, Films, Implant

Four participants in group
- * Photo
- * Etch
- * Diffusion
- * Films, Implant

Five participants in group
- * Photo (2)
- * Etch
- * Diffusion
- * Films, Implant

Six participants in group
- * Photo (2)
- * Etch
- * Diffusion
- * Films
- * Implant

Transistor Model Kit Contents & Materials



Transistor Model Kit Contents

Parts Inventory List
6 module nameplates
Set of 5 clear (acetate) photomasks
1 Run Card
8 bags of blocks (labeled by module)
baseplate (substrate)
1 Photo tool (flashlight)

*Make sure there are eight bags of parts.

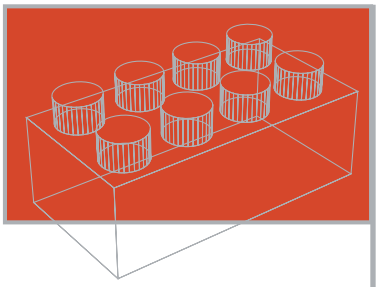
- Photoresist (Photo)
- Silicon Nitride (Diffusion)
- Field Oxide (Diffusion)
- Gate Oxide (Diffusion)
- Implant
- Polysilicon (Diffusion)
- Top Nitride (Films)
- Metal (Films)

Things to Check

1. Distribute the 6 module nameplates according to how many people will be working this lab.
3. Distribute the set of 5 photomasks (transparencies) to the photo operator.
4. Distribute the 8 bags of blocks to their respective modules (as indicated on the Parts Inventory List).
5. The color code used for each block as well as the number of different sizes of blocks is listed on your Parts Inventory List. (Use only if you think you're missing pieces or you want to duplicate this inventory for others.)
6. Double check to make sure you have your small flashlight as well as the green baseplate.
7. Pass the Run Card to the diffusion operator, since diffusion (as listed on the run card) is the first module scheduled to do work on the transistor.

Module Specific Duties

These are the names of the different manufacturing modules that the substrate will travel through toward becoming a transistor. This is a summary of the different instructions to be followed at each of the modules by the assigned operator. Please take a moment to read the instructions related to your assigned module. If you don't understand any module's duties, now would be a good time to ask your instructor.



Photolithography (4 steps)

1. Dispense photoresist (follow pattern on photoresist dispense template).
2. Align the mask.
3. Expose the wafer with light source.
4. Develop to remove exposed areas.

Thin Films (dielectric & metals)

Use the template as an aid for film deposition.

This is done to facilitate the etch process.

Etch

Remove material unprotected by photoresist.

Remove photoresist and return pieces to Photo.

Ion Implant

Implant material underneath areas unprotected by photoresist.

Remove photoresist and return pieces to Photo.

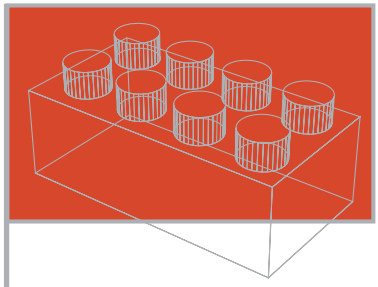
Diffusion

Use the template as an aid for film deposition.

This is done to facilitate the etch process.

***NOTE:** A short explanation of each manufacturing module is provided on pages 59 and 60. A glossary of terms is also available beginning on page 61.

Module Specific Duties



1. Photolithography
2. Thin Films (dielectric & metals)
3. Etch
4. Ion Implant
5. Diffusion

Question #2 / Matching

Match the numbered part above with the corresponding lettered answer.

____

____

____

____

____

A. Deposits thick layers of material on the transistor; usually requires more time and really hot furnaces.

B. Deposits thin layers of material on the transistor; generally requires less time, does not use furnaces, but does use specially designed tools.

C. Process of removing material unprotected by photoresist.

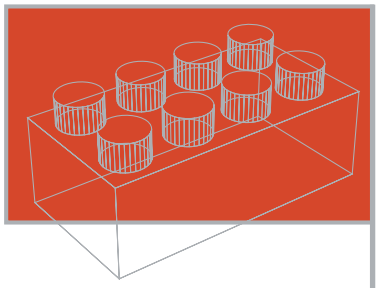
D. Involves a 4-step process of dispensing photoresist, aligning a mask, exposing the wafer with UV light, then developing the wafer to remove exposed photoresist.

E. Imbeds material underneath areas unprotected by photoresist.

Answers: A-5, B-2, C-3, D-1, E-4

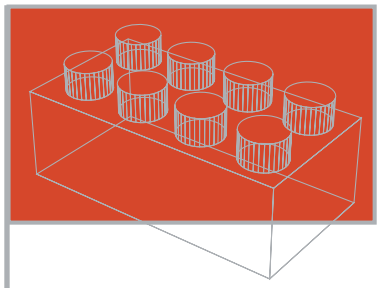
Transistor Run Card

Module	#	Operation	Initial	IN Time	Date		Initial	OUT Time	Date
Diffusion	100	Nitride Mask Deposition							
Photo	110	Field Ox Mask: 4 steps							
Photo	115	FOx Develop Inspection							
Etch	120	FOx Nitride Etch							
Etch	125	FOx Plasma Resist Strip							
Diffusion	200	Field Oxidation							
Diffusion	210	Nitride Mask Strip							
Diffusion	300	Gate Oxidation							
Diffusion	400	Polysilicon Deposition							
Photo	410	Poly Gate Mask: 4 steps							
Photo	415	PG Mask Defect Inspection							
Etch	420	PG Etch							
Etch	423	PG Plasma Resist Strip							
Etch	425	HF Residual GOx Clean							
Photo	510	N+ Source/Drain Imp Mask							
Photo	515	N+ S/D Imp DI							
Implant	520	N+ S/D Imp							
Implant	525	N+ S/D Plasma Strip (PS)							
Thin Films	600	Top Nitride Deposition							
Photo	610	Contact Mask: 4 steps							
Photo	615	Contact Defect Inspection							
Etch	620	Contact Etch							
Etch	625	Contact Resist Strip							
Thin Films	700	Metal Deposition							
Photo	710	Metal Mask: 4 steps							
Photo	715	Metal Defect Inspection							
Etch	720	Metal Etch							
Etch	725	Metal Resist Strip							
Etch	750	Final Inspection							

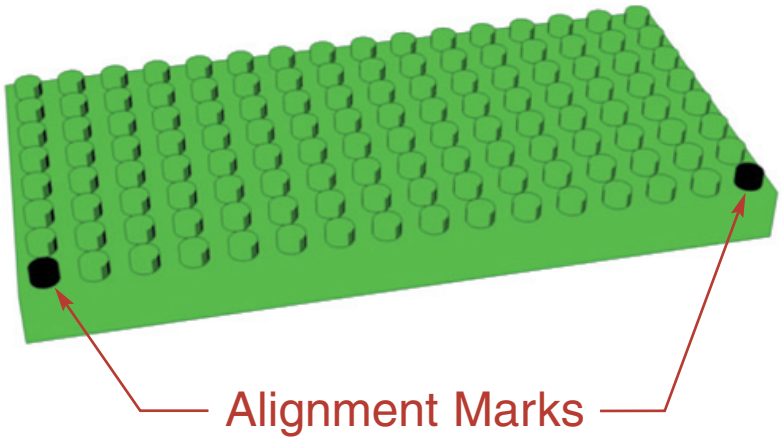


The Run Card is used in this simulation to represent several things. First, it tracks the movement of a wafer through the different modules that it visits during the fabrication of a transistor. Second, it leaves a trail of its stages of development in order to backtrack problem areas to correct them or to backtrack high-success areas to recreate them. This tracking system is so in-depth that a single product's history can be traced back to the silicon from which it was created. In this simulation, the Run Card will follow the movement of the product to the five different modules to indicate the type of work needed to be done. The operator who performs the work on the product needs to initial the Run Card as well as indicate the date and time that the wafer was received into the module (the same for when the wafer exited the module). This information, together with the ID of the product itself, is what generates the data trail. In an actual fab, this process is substantially computerized.

Transistor Model Assembly Procedure



Substrate



Objective: Inspect the silicon substrate and qualify it as fit for production.

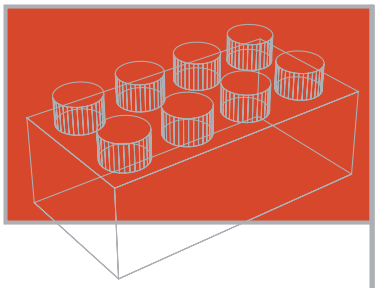
Purpose: Constructing a replica of the transistor starts with its silicon substrate (or base). This substrate will support several layers that will be added to it, the layers themselves comprising the structures of the different elements of the transistor.

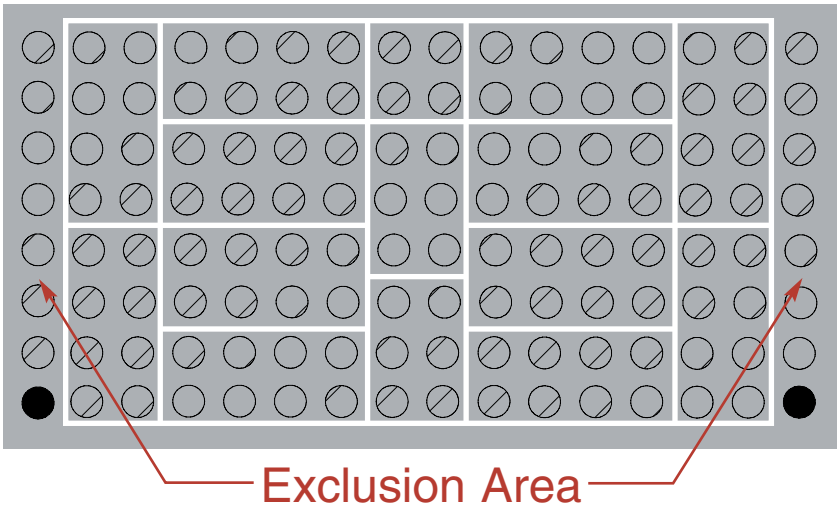
Background: In regards to size, the thickness of the building block base is 1 cm, whereas the thickness
of an actual transistor substrate is 10 times smaller (1 mm, or close to the thickness of a dime). The length of the building block base is around 12 cm, whereas an actual transistor length is around 2 million times smaller, or 5 micrometers (0.000005 m). Finally, the depth of the silicon substrate (building block base) is around 6 cm, whereas the actual transistor depth is around 1 million times smaller, or 5 micrometers (about the same distance as the transistor's length).

Procedure: Locate the green base plate. This is the substrate for the transistor. Inspect it. Note the two alignment marks as well as the front and rear of the substrate. The front of the substrate will be considered to be where the alignment marks are located.

Nitride Mask Deposition Template

Diffusion





Objective: The next 10 steps (#'s 100 – 210 on the Run Card) will result in the formation of field oxide (a barrier wall) around the perimeter of the transistor. Deposit nitride blocks onto the substrate as shown on the nitride deposition template.

#	Operation	Module	Equipment	Physical	Chemical
100	Nitride Mask Deposition	Diffusion	Low Pressure Chemical Vapor Deposition Furnace (LPCVD)	High temperature (~750° C), low pressure (~200 mtorr), gas flow rate, time	Dichlorosilane + Ammonia → $3SiCl_2H_2$ + $4NH_3$ ---------- Silicon Nitride + Byproducts Si_3N_4 + $(6HCl + 6H_2)$

Purpose: A thin, protective layer of silicon nitride is deposited on the surface of the wafer. The nitride will serve as a hard mask layer during the field oxidation process.

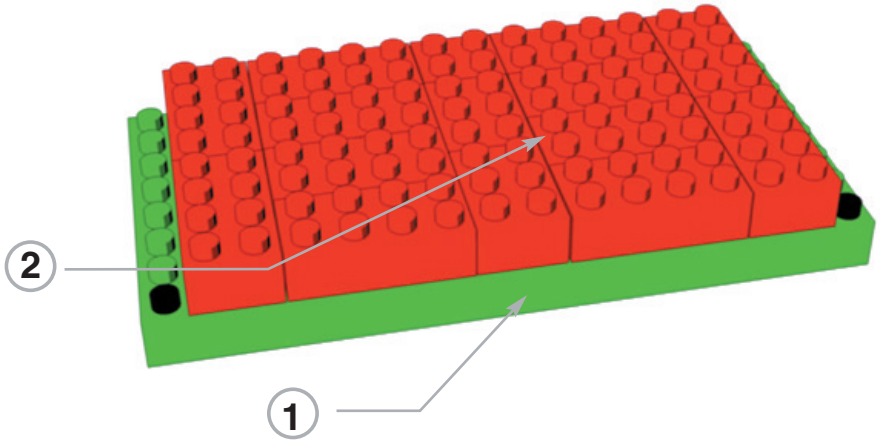
Procedure: Using the nitride mask template, place the red (nitride) blocks over the surface of the green base plate (substrate). Note also that no blocks are placed on the outer columns. These columns are referred to as exclusion areas.

[Remember to fill out the Run Card]

Nitride Deposition Assembly

1	Substrate
2	Silicon Nitride
ADD	12 2x4
	2 2x3
	1 2x2

Diffusion



This slide illustrates what the nitride layer will look like when deposition of silicon nitride has been completed.

Question #3

What purpose does the nitride layer serve?

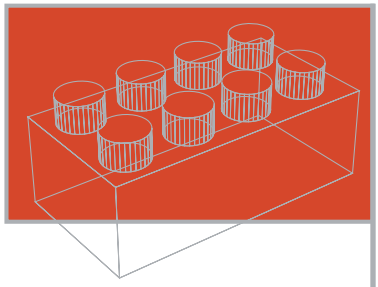
A. The nitride layer acts as an insulating material that isolates the transistor from other components of a larger integrated circuit.
B. The nitride layer acts as a thin film that serves as a mask layer during the field oxidation process.
C. The nitride layer, when exposed to light, becomes grainy and soluble and can be removed by a solvent.
D. The nitride layer is a semiconductive material that forms the foundation of the transistor.

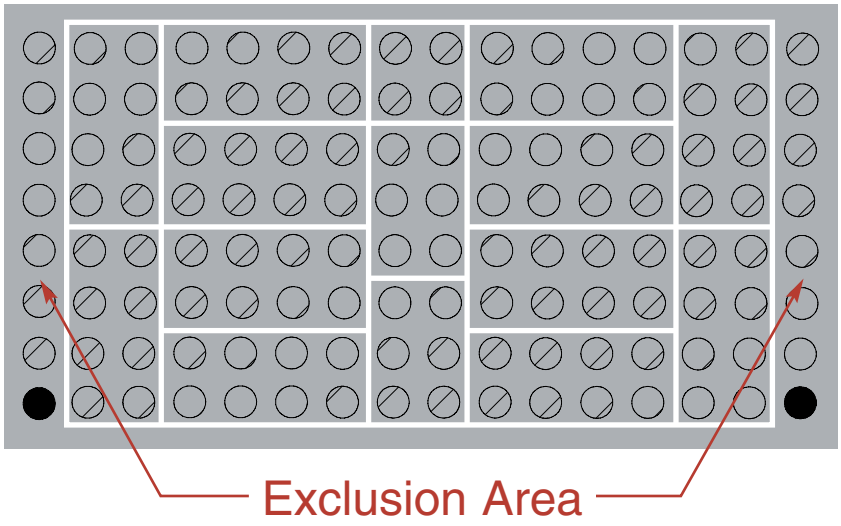
Answer: B

[Remember to fill out the Run Card]

Photoresist Dispense Template

Photo





Objective: Dispense photoresist onto the substrate as shown on the photoresist dispense template.

#	Operation	Module	Equipment	Physical	Chemical
110A	(FOx) Photoresist Dispense	Photo	Coater / Developer	Dispense quantity, spin speed, spin time	Photoresist (a light-sensitive material)

Purpose: This is the first of four operations in the photo process. Photoresist, a liquid photographic film, is deposited on the wafer in photolithography. Typically, photoresist is dispensed onto a spinning wafer to spread it evenly across the surface. The substrate is then baked to improve the adhesion of the photoresist to the substrate (represented later by how hard you will find it to take the building blocks apart). Also, the baking process helps to further spread out the photoresist evenly over the substrate's surface.

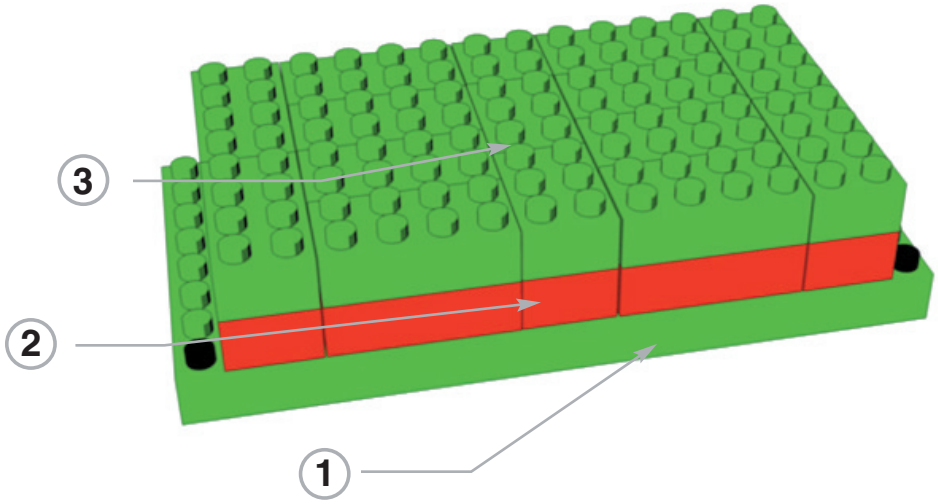
Procedure: Place the green photoresist blocks over the surface of the transistor, except for the exclusion zone. Follow the pattern indicated on the photoresist dispense template, as this will make it easier to perform the operations that follow on your substrate.

[Remember to fill out the Run Card]

Photoresist Dispense Assembly

1	Substrate
2	Silicon Nitride
3	Photoresist
ADD	12 2x4
	2 2x3
	1 2x2

Photo



This slide illustrates what the photoresist layer will look like when you are finished dispensing and photoresist has been completed.

Question #4

What purpose does the photoresist layer serve?

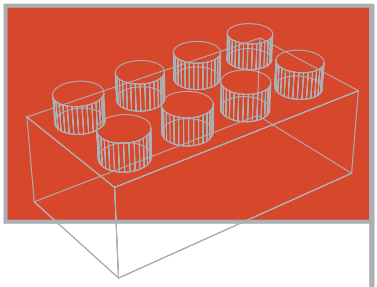
A. The photoresist layer acts as an insulating material that isolates the transistor from other components of a larger integrated circuit.
B. The photoresist layer acts both as a thin film that protects the transistor from contamination and as a mask layer.
C. The photoresist layer is a liquid photographic film used in the photolithography process.
D. The photoresist layer is a semiconductive material that forms the foundation of the transistor.

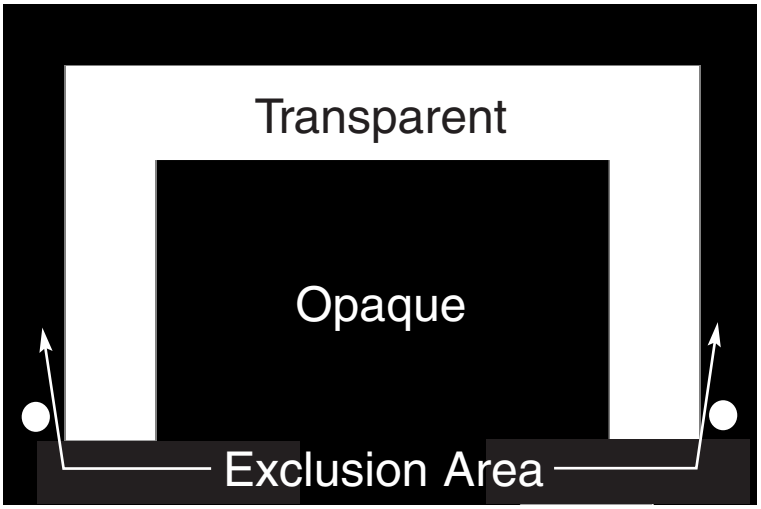
Answer: C

[Remember to fill out the Run Card]

Nitride Mask (Align & Expose)

Photo





Objective: The nitride mask (used to define the location of the field oxide wall) is aligned on top of the substrate before photoresist is exposed to UV light through the transparent opening of the mask.

#	Operation	Module	Equipment	Physical	Chemical
110B	Align mask	Photo	Stepper: Aligns substrate to the mask pattern.	Alignment accuracy is critical.	N/A
110C	Expose	Photo	Stepper: Uses UV light to expose photoresist	The wafer is exposed to UV light. Energy and time of exposure are main parameters.	Photoresist (a light-sensitive material) that becomes acidic when exposed to UV light

Purpose: The substrate must be accurately aligned to the mask pattern. The transparent area of the mask allows light from the stepper to expose specific areas of the photoresist-coated substrate. In the case of positive-type photoresist, the kind used in this simulation, it is the exposed photoresist that undergoes a chemical change.

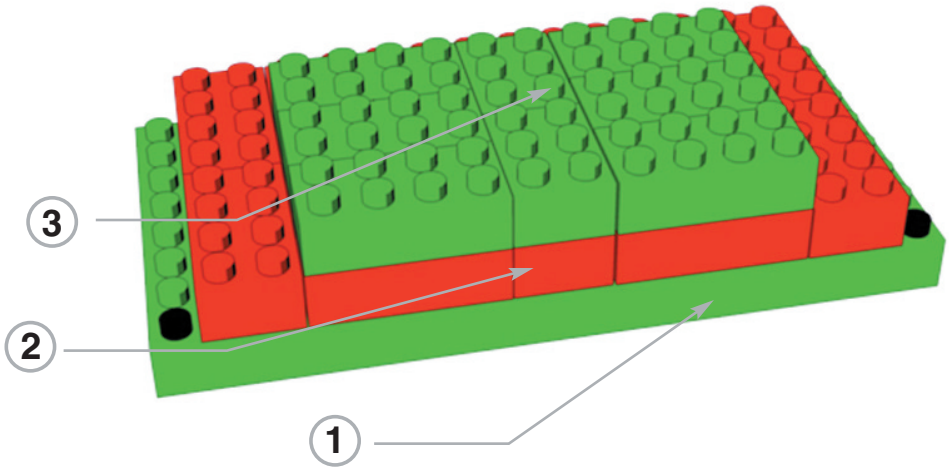
Procedure: Place the nitride mask over the green base plate. Use the alignment marks to ensure accurate placement. Shine the flashlight through the mask and notice the green photoresist blocks that are exposed to light.

[Remember to fill out the Run Card]

Nitride Mask Resist Develop

1	Substrate
2	Silicon Nitride
3	Photoresist
SUBTRACT	6 2x4
	1 2x2

Photo



Objective: Remove the photoresist blocks that were exposed to the light.

#	Operation	Module	Equipment	Physical	Chemical
110D	Develop to remove exposed photoresist	Photo	Coater / Developer	Dispense quantity, time, temperature, rinse, and spin speed	Exposed photoresist becomes acidic and is removed with a develop chemical by neutralizing its acidity.

Purpose: The purpose of the develop step is to chemically remove the photoresist that was exposed to UV light. The result of this develop process is to selectively uncover areas of the nitride that are to be removed during the etch operation.

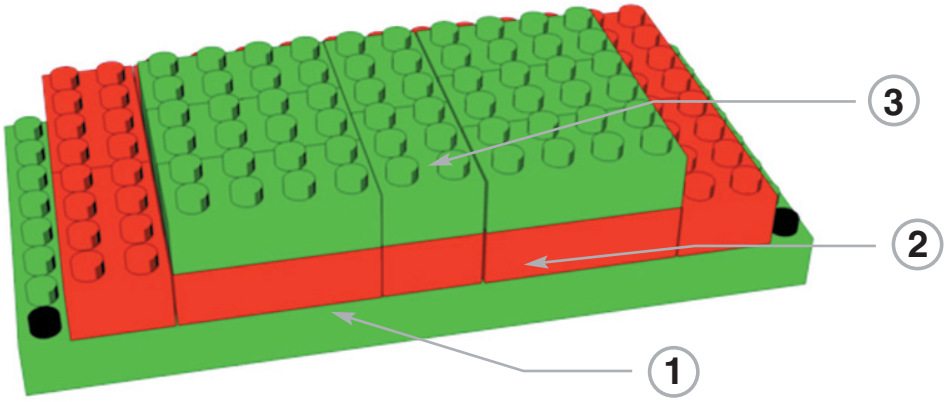
Procedure: From the previous step, remove only those blocks of photoresist that were exposed to light from the flashlight. These blocks should form the shape of a cut-out "U" around the perimeter of the transistor.

[Remember to fill out the Run Card]

Nitride Mask Defect Inspect

Photo

1	Substrate
2	Silicon Nitride
3	Photoresist



Objective: Inspect the photoresist removed in the develop process. This is done to make sure that the field oxide's location is where it should be.

#	Operation	Module	Equipment	Physical	Chemical
115	FOx Develop Inspection	Photo	Optical Microscope	Inspect the site of removed photoresist	N/A

Purpose: In Defect Inspection (DI), make sure that everything is where it's supposed to be, that the photoresist removed in the previous step was exactly the photoresist that was supposed to be removed: No more and no less (given specific tolerances for error). If not, all photoresist can be stripped from the wafer and reapplied to be exposed and developed again. Photolithography is the only part of wafer manufacturing that can be reworked if a mistake is made.

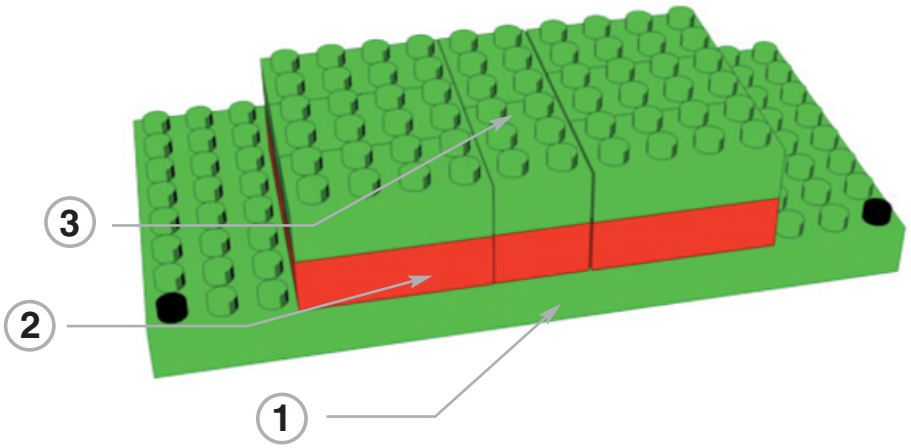
Procedure: Place the transparency mask over the model. Ensure that there are no photoresist blocks underneath the clear areas of the mask. The only place on the model where photoresist blocks should be found is directly underneath the dark areas of the mask.

[Remember to fill out the Run Card]

Nitride Etch

1	Substrate
2	Silicon Nitride
3	Gate Oxide
SUBTRACT	 6 2x4
	 1 2x2

Etch



Objective: All nitride that is not protected by photoresist is etched away.

#	Operation	Module	Equipment	Physical	Chemical
120	FOx Nitride Etch	Etch	Dry Plasma Etcher	High-powered radio-frequency energy ionizing a gas inside a vacuum makes it easy to remove unwanted silicon nitride.	Fluorine- or chlorine-based gases become highly reactive when ionized.

Purpose: The etching process selectively removes the nitride that was unprotected by photoresist. A large area of nitride remains to form a protective mask layer over a portion of the silicon substrate.

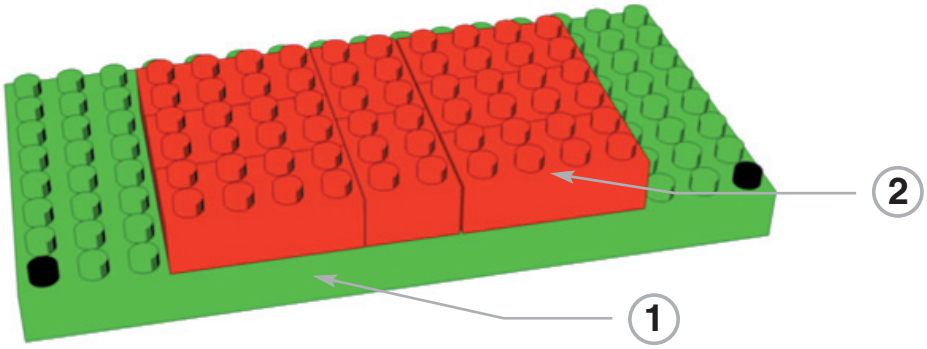
Procedure: Remove the red (nitride) blocks that are not covered by the green (photoresist) blocks straight down to the green base plate (silicon substrate). Return the red blocks to the Diffusion module.

[Remember to fill out the Run Card]

Resist Strip

Etch

1	Substrate
2	Silicon Nitride



Objective: Remove all remaining photoresist.

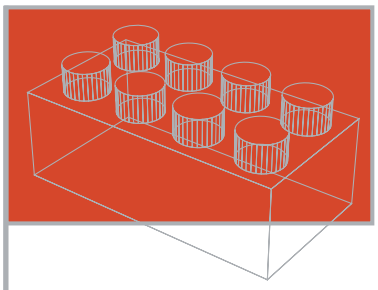
#	Operation	Module	Equipment	Physical	Chemical
125	FOx Plasma Resist Strip	Etch	Dry Plasma Etcher	RF power, chamber pressure, gas flow, temperature, time	Ionized oxygen is used to remove the photoresist.

Purpose: This second step in the etch process gets rid of all remaining photoresist so that only the nitride layer remains.

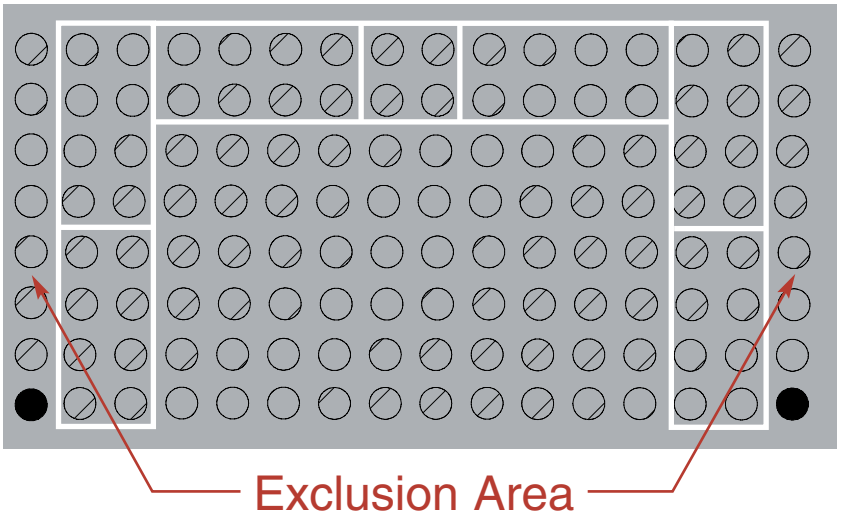
Procedure: Remove the green blocks of photoresist from on top of the red (nitride) blocks, and return the green blocks to the Photo module.

[Remember to fill out the Run Card]

Field Oxide Template



Diffusion



Objective: Attach field oxide above and below the substrate as shown on the field oxide template. Silicon dioxide is now grown around the boundary of the transistor wherever nitride is not present.

#	Operation	Module	Equipment	Physical	Chemical
200	Field Oxidation	Diffusion	High-temperature furnace	Temperature: (~1000° C), gas flow, time.	Silicon + Oxygen → Silicon Dioxide Si O_2 SiO_2

Purpose: This template shows where oxygen will grow. Oxygen, the only chemical element introduced at this stage, will only combine with the silicon. Oxygen will not combine with the nitride layer that was previously placed. The oxygen will form silicon dioxide ("glass" or "oxide") only where silicon is exposed. Chemically, this process is referred to as oxidation, or that the oxidizing of silicon produces silicon dioxide, or just "glass." When oxygen combines with other materials, such as iron, the oxidation of iron produces iron oxide, or just "rust."

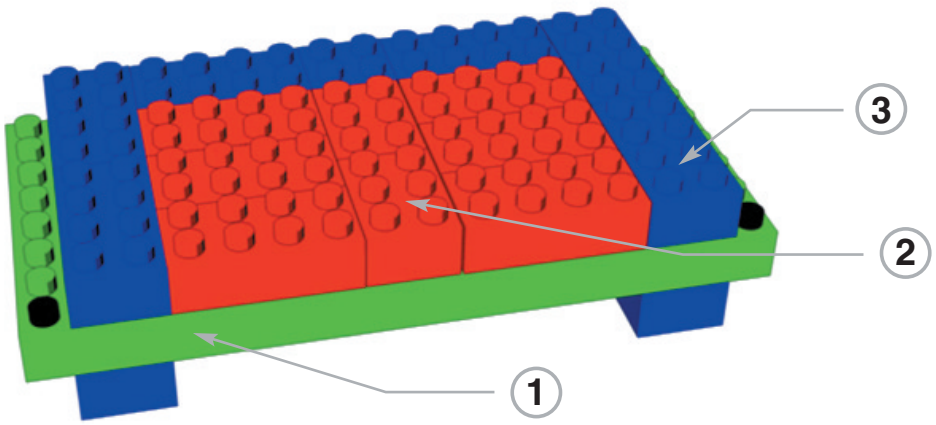
Procedure: Use the field oxide template to place the blue field oxide blocks on the transistor. They will arrange themselves around the outside perimeter of the red silicon nitride blocks. When done correctly, the field oxide should be attached above and below the substrate as shown on the field oxide template.

[Remember to fill out the Run Card]

Local Oxidation of Silicon

Diffusion

1	Substrate
2	Silicon Nitride
3	Silicon Dioxide
ADD	12 2x4
	2 2x2



This slide illustrates what the field oxide will look like when it is finished growing on the silicon substrate, forming the field oxide. Local oxidation of silicon (LOCOS) is the name of the process that has been used for many years to selectively grow silicon dioxide in areas of silicon that are unprotected by the silicon nitride mask. In reality, oxidation occurs in all directions of the exposed silicon. The model shows oxide growing vertically through the silicon. The model does not, however, demonstrate the horizotal growth of the oxide.

Question #5

What purpose does the local oxidation of silicon (LOCOS) serve?

A. LOCOS is the formation of the field oxide layer, which acts as an insulating material isolating the transistor from other components of a larger integrated circuit.
B. LOCOS is a positively charged material because it has a deficiency of electrons.
C. LOCOS, when exposed to light, becomes grainy and soluble and can be removed by a solvent.
D. LOCOS is a semiconductive material that forms the foundation of the transistor.

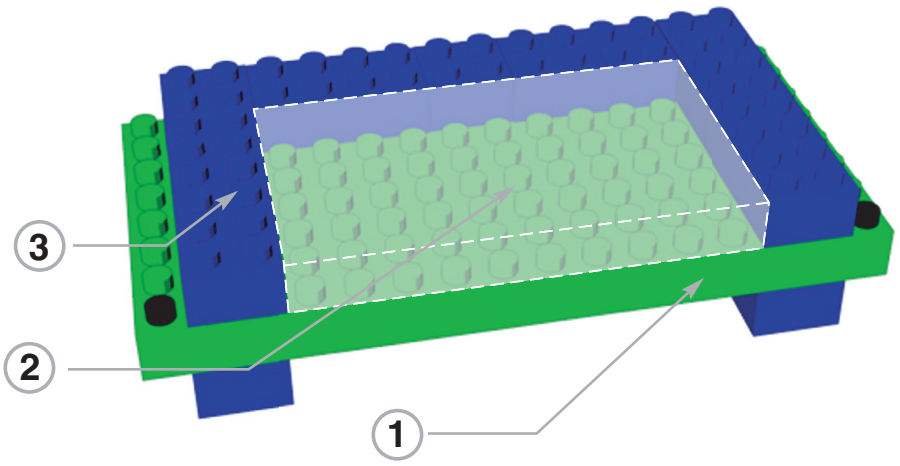
Answer: A

[Remember to fill out the Run Card]

Nitride Strip

1	Substrate
2	Removed Nitride
3	Silicon Dioxide
SUBTRACT	6 2x4
	2 2x3

Diffusion



Objective: Ensure the remaining nitride is removed from the transistor.

#	Operation	Module	Equipment	Physical	Chemical
210	Nitride Mask Strip	Diffusion	Acid bath	Temperature, time rinse, and dry	Phosphoric acid is used to strip the silicon nitride.

Purpose: This is the last stage of forming the field oxide. The blue wall is now clearly evident around the perimeter of the transistor area. The electrical components of this transistor can now be isolated from neighboring electrical components. Even though the process took 11 steps in this simulation to create the field oxide for one transistor, this same process is duplicated on all transistors being manufactured on a real silicon substrate.

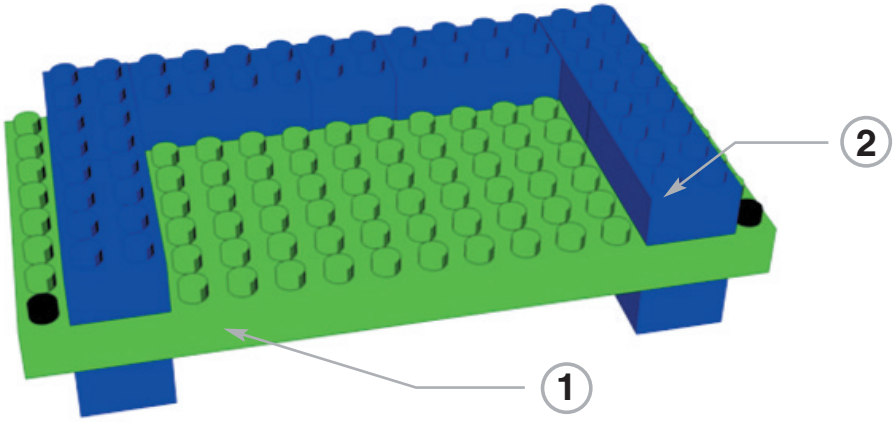
Procedure: Remove the red (nitride) blocks during this stage. Return the red blocks to the Diffusion module.

[Remember to fill out the Run Card]

Nitride Strip

Diffusion

1	Substrate
2	Silicon Dioxide



Question #6

The process of making field oxide took 10 steps. Which of the following would be a correct sequence of steps?

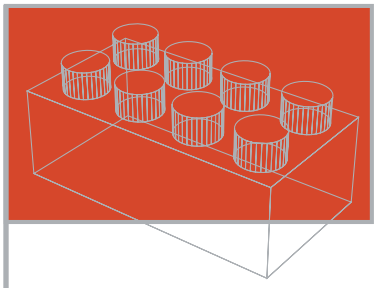
1. Used a combination of photo and etch to pattern the nitride.
2. Deposited nitride over the entire substrate.
3. Used oxidation to form the field oxide around the nitride.
4. Used phosphoric acid to strip off the nitride.

A. 4, 3, 2, 1
B. 3, 4, 1, 2
C. 1, 3, 4, 2
D. 2, 1, 3, 4

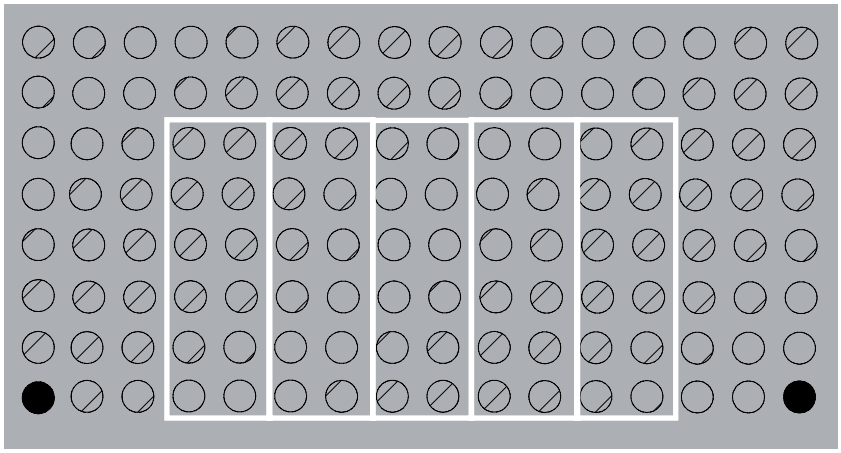
Answer: D

[Remember to fill out the Run Card]

Gate Oxide Template



Diffusion



Objective: The next 10 steps (#'s 300 – 425 on the Run Card) will result in the formation of the transistor's gate. The first step in this process will be to lay down dielectric material, a thin oxide layer, over the whole surface of the substrate.

#	Operation	Module	Equipment	Physical	Chemical
300	Gate Oxidation	Diffusion	Oxidation furnace	Temperature, time (critical as contamination here is easy).	Oxygen is introduced into this furnace to grow a thin layer of oxide.

Purpose: Gate oxide will serve as dielectric material separating the gate electrode from the substrate. This part in the process of making a transistor is one of the most critical because the film is so thin — less than 100 angstroms (Å). To get a comparison of this size, look up in the glossary under angstrom and see what the diameter of human hair is in angstroms. Temperature and the amount of oxygen the silicon is exposed to are very important. However, more important is the length of time the silicon is exposed to oxygen. Even when exposed to open air, the silicon oxidizes. Since the gate oxide film is so thin, contamination control is very important.

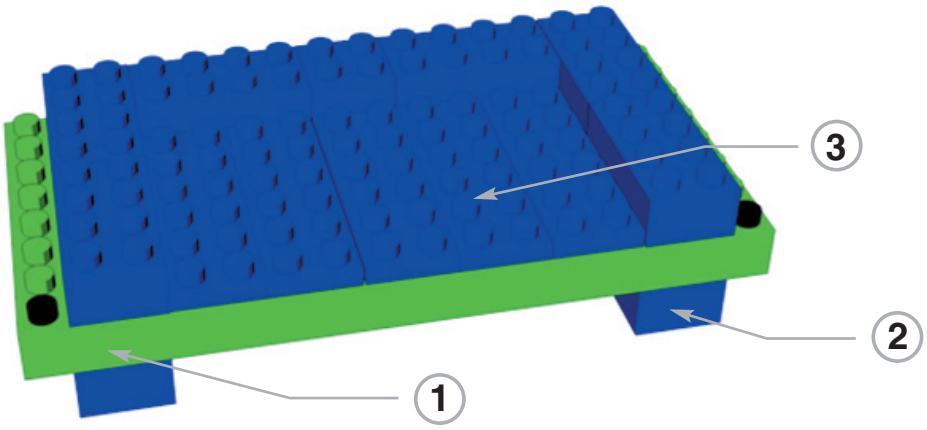
Procedure: Place the thin plates of gate oxide (blue plates) on top of the substrate following the pattern on the gate oxide template.

[Remember to fill out the Run Card]

Gate Oxidation

Diffusion

1	Substrate
2	Silicon Dioxide
3	GateOxide
ADD	5 2x6



This slide illustrates what the wafer should look like after the gate oxide has been placed on top of the transistor following the gate oxide template.

Question #7 / Matching Review

Match the numbered description with the corresponding lettered answer.

1. Soluble material that can be removed by develop chemical.
2. A light-sensitive chemical used in the patterning process of wafer fab.
3. This chemical process is similar to the rusting of iron.
4. The manufacturing of a MOS transistor begins with this.
5. A form of energy used in exposure of photoresist.

Answer: 1-C, 2-A, 3-D, 4-E, 5-B

A. Photoresist

B. Ultraviolet Light

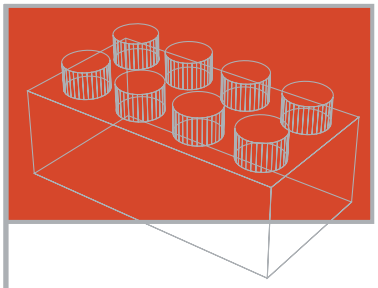
C. Exposed areas of photoresist

D. Oxidation

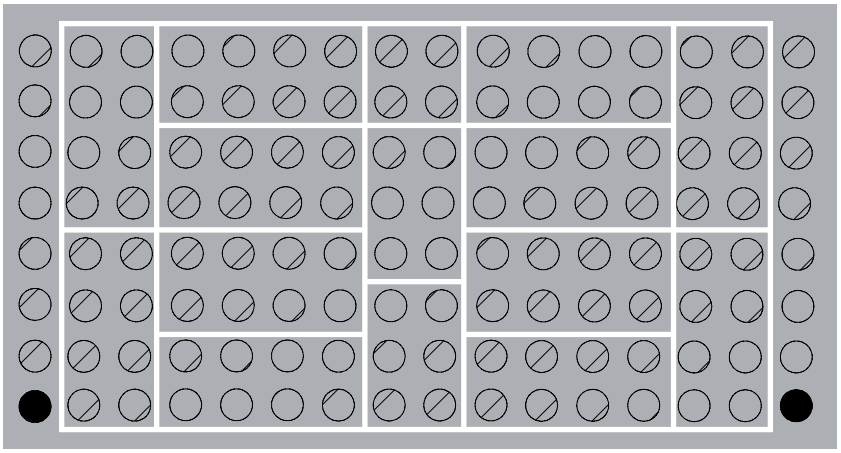
E. Silicon substrate

[Remember to fill out the Run Card]

Polysilicon Gate Template



Diffusion



Objective: Deposit polysilicon over the top surface according to the pattern shown on the polysilicon gate template.

#	Operation	Module	Equipment	Physical	Chemical
400	Polysilicon Gate Deposition	Diffusion	Low Pressure Chemical Vapor Deposition Furnace (LPCVD)	High temperature, low pressure, time	(Heat) Silane gas SiH_4 → Polysilicon + Hydrogen Si $2H_2$

Purpose: Polysilicon (basically the same semiconductive material as silicon) is deposited on the substrate as a result of the decomposition of silane (SiH_4) gas in a high-temperature/low-pressure furnace. The silicon deposits on the substrate and accumulates like snowflakes falling on the ground. The purpose of the polysilicon is to serve as the material from which the transistor's gate electrode is formed.

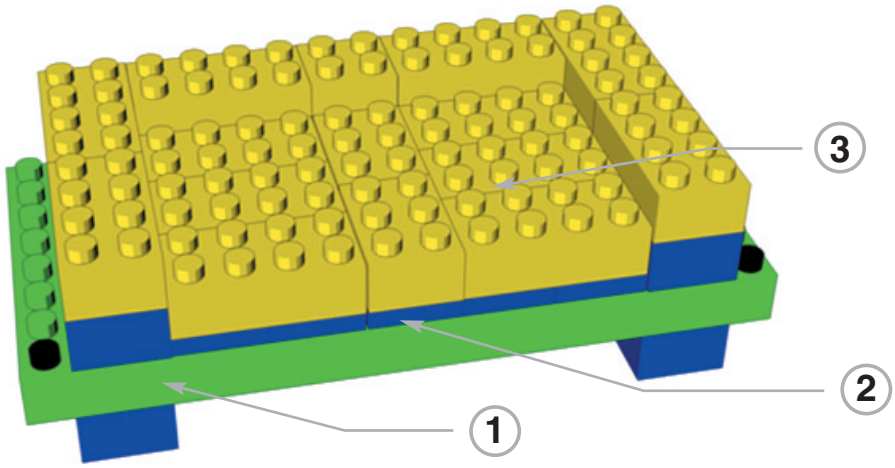
Procedure: Place the yellow blocks (polysilicon) over the top surface of the transistor following the polysilicon gate template.

[Remember to fill out the Run Card]

Polysilicon Gate Deposition

Diffusion

1	Substrate
2	GateOxide
3	Polysilicon
ADD	12 2x4
	2 2x3
	1 2x2



This slide illustrates what the wafer should look like after the layer of yellow blocks representing polysilicon has been distributed over the top surface of the wafer.

Question #8

Which statement is true about the polysilicon layer?

A. The polysilicon layer acts like the dielectric of a capacitor that can store a charge.
B. The polysilicon layer's dimensions are the thinnest in the transistor.
C. The polysilicon layer will serve as the material from which the gate is formed.
D. The polysilicon layer, when exposed to light, becomes grainy and soluble and can be removed by a solvent.

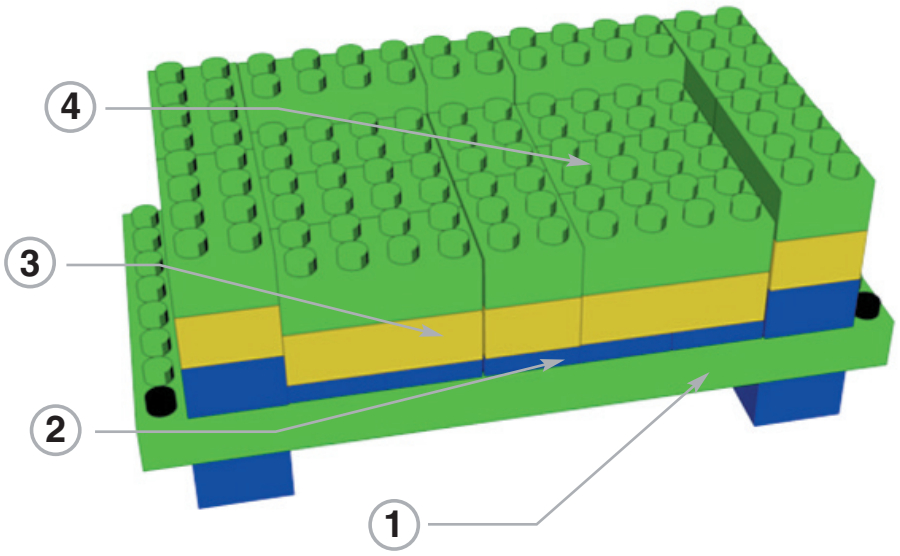
Answer: C

[Remember to fill out the Run Card]

Polysilicon Gate Resist Dispense

1	Substrate
2	Gate Oxide
3	Polysilicon
4	Photoresist
ADD	12 2x4
	2 2x3
	1 2x2

Photo



Objective: Deposit photoresist on the substrate to match the pattern shown on the photoresist template.

#	Operation	Module	Equipment	Physical	Chemical
410A	Polysilicon Gate Mask Photoresist Dispense	Photo	Coater / Developer	Dispense quantity, spin speed, spin time	Photoresist (a light-sensitive material)

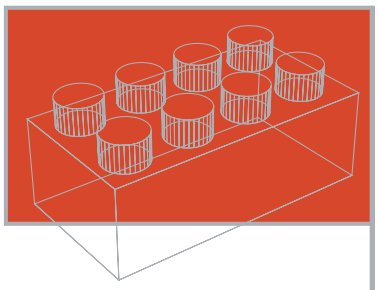
Purpose: This represents the first step in photolithography to transfer the pattern of the gate onto the transistor. Photoresist is dispensed over the surface of the wafer to capture the image of the polysilicon gate mask after exposure to UV light.

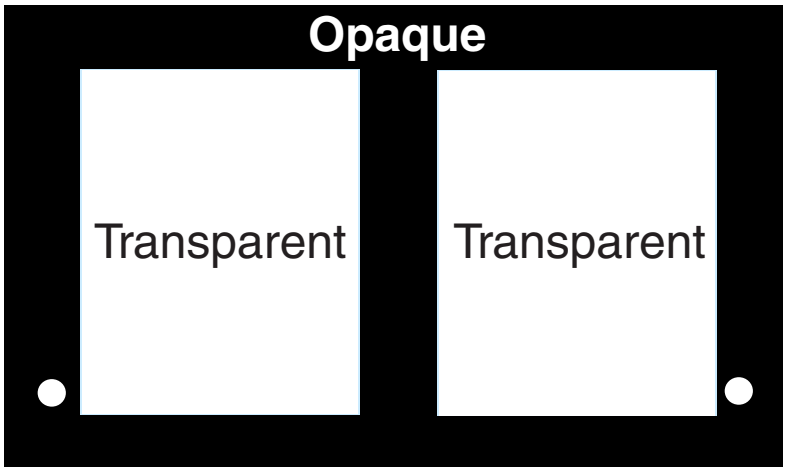
Procedure: Place the green photoresist blocks over the surface of the transistor. Follow the pattern indicated on the photoresist dispense template, as this will make it easier to perform the following operations on the substrate.

[Remember to fill out the Run Card]

Nitride Mask (Align & Expose)

Photo





Objective: The gate mask is aligned on top of the wafer in the Photo module.

#	Operation	Module	Equipment	Physical	Chemical
410B	Align Mask	Photo	Stepper: Aligns substrate to the mask pattern.	Alignment accuracy is critical.	N/A
410C	Expose	Photo	Stepper: Uses UV light to expose photoresist.	The wafer is exposed to UV light. Energy and time of exposure are main parameters.	Photoresist (a light-sensitive material) that becomes acidic when exposed to UV light

Purpose: This represents the second and third step in Photo to make the gate. The mask is aligned over the substrate, then those areas under the transparent parts of the mask are exposed to ultraviolet light. As the pattern of the mask indicates, most of the photoresist except for the thin strip down the middle (the location of the gate), will be removed during the fourth step in Photo, in the develop stage. Typically, it is the ability of the camera system to transfer the pattern of the gate through photolithography that limits the operation of the transistor. The width of the gate (currently at the 0.18 micron level), determines the operating speed of the transistor.

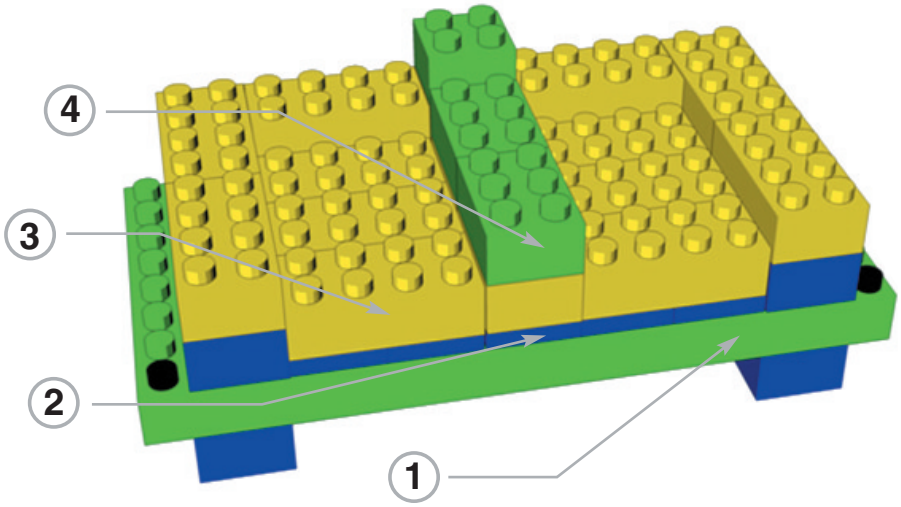
Procedure: Place the poly gate mask over the transistor using the alignment marks. Shine the flashlight through the mask and notice the green photoresist blocks that are exposed to light.

[Remember to fill out the Run Card]

Poly Gate Resist (Develop & Inspect)

1	Substrate
2	Gate Oxide
3	Polysilicon
4	Photoresist
SUBTRACT	 12 2x4

Photo



Objective: Remove the photoresist blocks that were exposed to the light. Then, inspect the photoresist that was removed to make sure that the gate's location is where it should be.

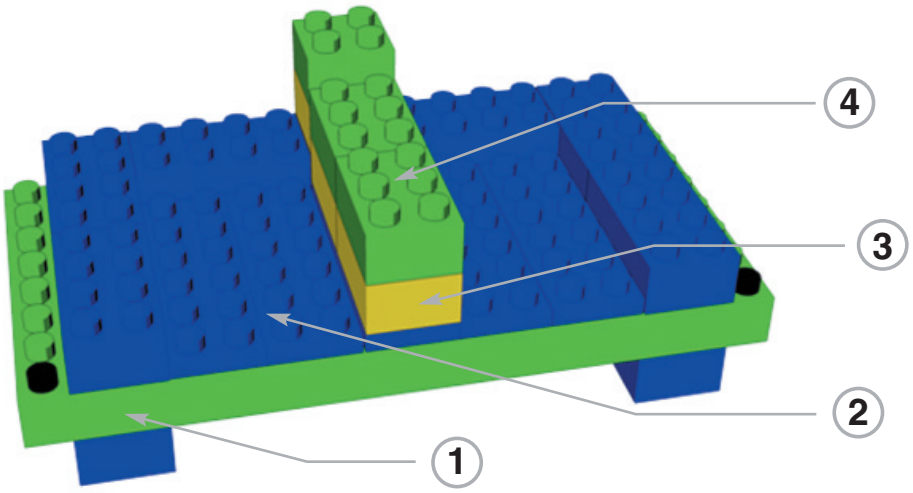
#	Operation	Module	Equipment	Physical	Chemical
410D	Polysilicon Gate Photoresist Develop	Photo	Coater / Developer	Dispense quantity, time, temperature, rinse, and spin speed	Exposed photoresist becomes acidic and is removed with a develop chemical by neutralizing its acidity.
415	Develop Inspect	Photo	Optical Microscope	Inspect the site of removed photoresist.	N/A

Purpose: The purpose of the Develop step is to chemically remove the photoresist that was exposed to UV light. The result of this develop process is to selectively uncover areas of polysilicon that are to be removed during the etch operation. In Defect Inspection (DI), make sure that the resist removed is supposed to be removed. If done correctly, any remaining photoresist should just be covering the location of the gate, which is very thin. Again, if there's a mistake made here, this step can be repeated after all resist is stripped away.

Procedure: From the previous step, remove only those green blocks of photoresist that were exposed to light from the flashlight. Return the green blocks to the Photo module. Then inspect the model to make sure that the blocks that were removed from the develop process were indeed the blocks that were supposed to be removed.

Poly Gate Etch

Etch



1	Substrate
2	Gate Oxide
3	Polysilicon
4	Photoresist
SUBTRACT	12 2x4

Objective: All polysilicon not protected by photoresist is removed.

#	Operation	Module	Equipment	Physical	Chemical
420	Poly Gate Etch	Etch	Dry Plasma Etcher	High-powered radio-frequency energy ionizing a gas inside a vacuum makes it easy to remove unwanted polysilicon.	Flourine- or chlorine-based gases become highly reactive when ionized.

Purpose: The etching process selectively removes the polysilicon that was unprotected by photoresist. This is a critical step in that the etching has to be done precisely so as to cut away only that portion of polysilicon material that will not form part of the gate structure.

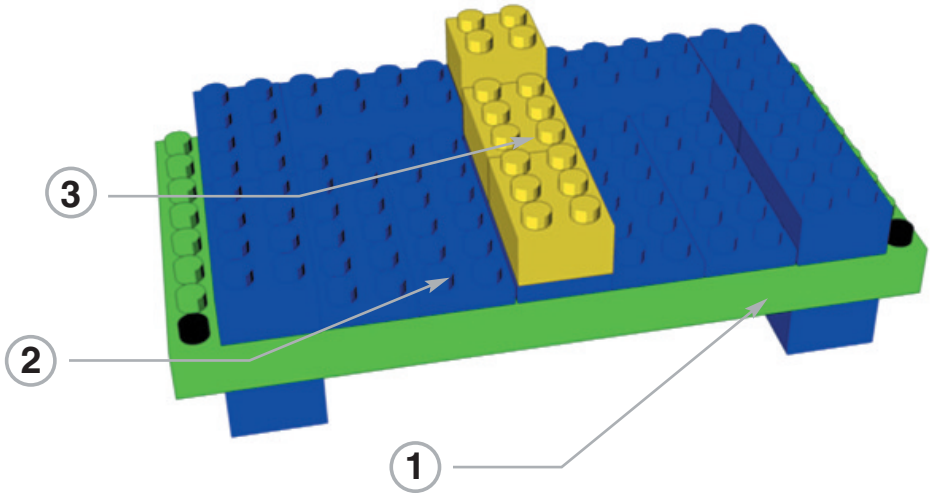
Procedure: Remove all yellow blocks of polysilicon that are not covered by the green blocks (photoresist). Return yellow blocks to the Diffusion module.

[Remember to fill out the Run Card]

Poly Gate Resist Strip

1	Substrate
2	Gate Oxide
3	Polysilicon

Etch



Objective: All remaining photoresist is removed at this stage.

#	Operation	Module	Equipment	Physical	Chemical
423	Polysilicon Gate Plasma Photoresist Strip	Etch	Dry Plasma Etcher	RF Power, chamber pressure, gas flow, temperature, time	Ionized oxygen is used to remove the photoresist.

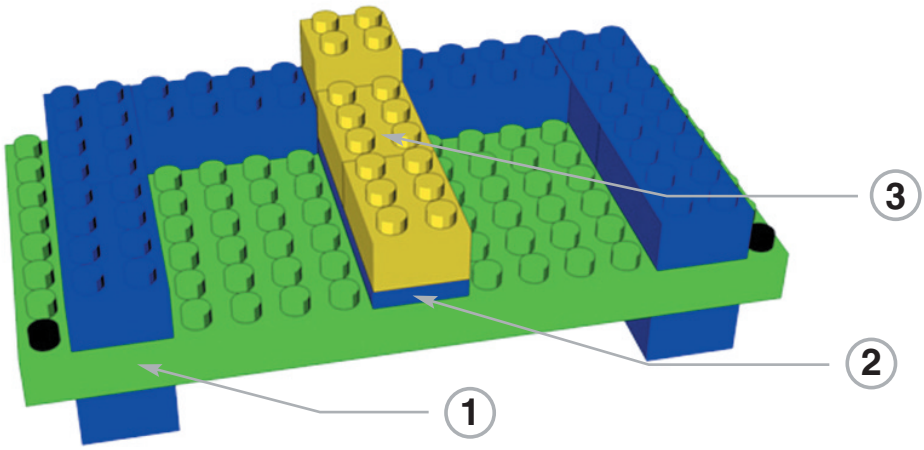
Purpose: In this operation, all remaining photoresist is removed. The only section of photoresist still remaining is the section over the gate structure.

Procedure: Remove the remaining green blocks of photoresist from on top of the gate structure. Return the green blocks to the Photo module.

[Remember to fill out the Run Card]

HF Residual Gate Oxide (GOx) Clean

Etch



1	Substrate
2	Gate Oxide
3	Polysilicon
SUBTRACT	4 2x6

Objective: Remove residual gate oxide.

#	Operation	Module	Equipment	Physical	Chemical
425	HF Residual GOx Clean	Etch	Wet Clean Station	Time, temperature	Buffered oxide etch, a solution of: $NH_4F + HF + H_2O$

Purpose: The purpose of this wet clean is to remove the residual gate oxide. A solution of ammonium fluoride (NH_4F), hydrofluoric acid (HF), and water (H_2O) form a buffered oxide etch (BOE) that removes this oxide. The oxide is very thin, so it doesn't take much time to perform this operation.

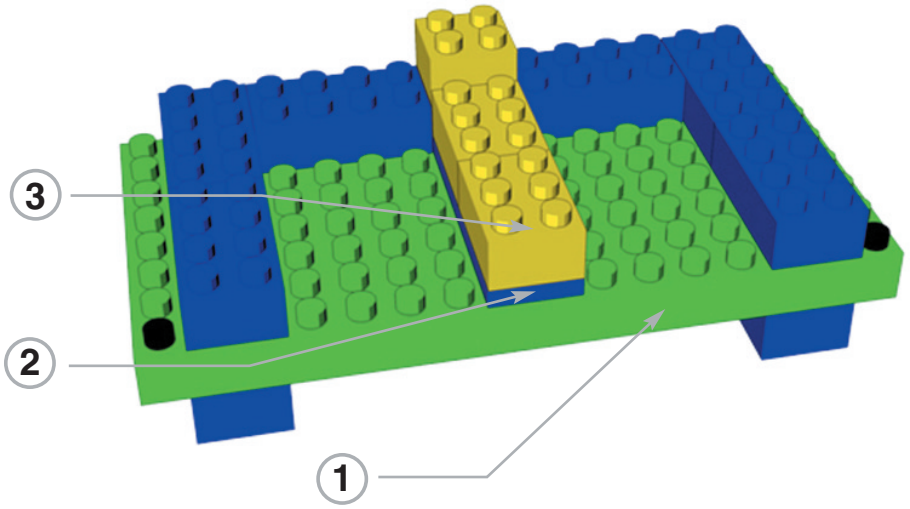
Procedure: Remove the blue (gate oxide) plates that are not covered by the yellow (polysilicon) blocks. Return the blue plates to the Diffusion module.

[Remember to fill out the Run Card]

Gate Structure End-Result

1	Substrate
2	Gate Oxide
3	Polysilicon

Etch



Question #9

The process of making the gate took 10 steps. Which of the following would be a correct sequence of steps?

1. The wafer is etched to remove all polysilicon not covered by photoresist, after which all remaining photoresist is removed.
2. Photoresist is dispensed on the wafer, after which it is exposed with UV light, then developed.
3. Polysilicon is deposited on top of the dielectric layer (gate oxide) of the wafer.
4. The unprotected gate oxide is removed with BOE.

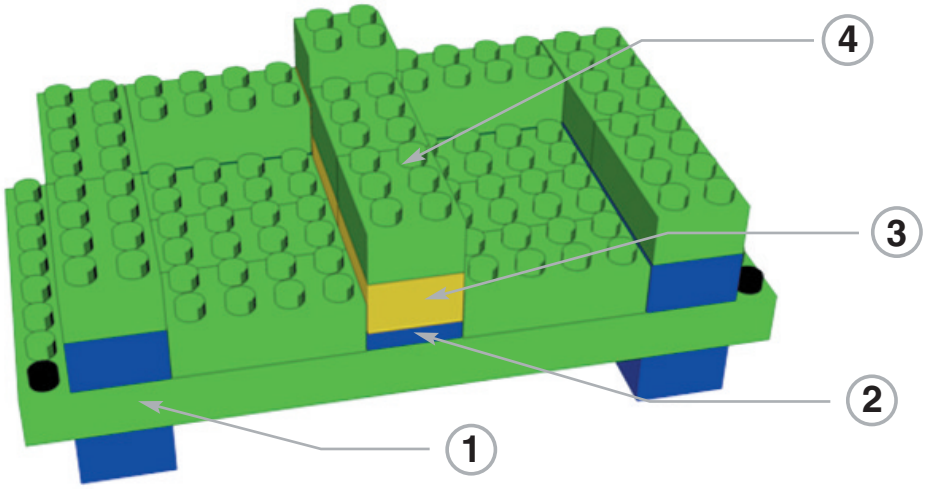
A. 4, 1, 2, 3
B. 3, 2, 1, 4
C. 2, 4, 1, 3
D. 3, 1, 4, 2

Answer: B

[Remember to fill out the Run Card]

Implant Mask
Resist Dispense

Photo



1	Substrate
2	Gate Oxide
3	Polysilicon
4	Photoresist
ADD	12 2x4
	2 2x3
	1 2x2

Objective: The next 7 steps (#'s 510 – 525 on the Run Card) will result in the formation of the source and drain of the transistor. The first step in this process begins with dispensing photoresist on the wafer.

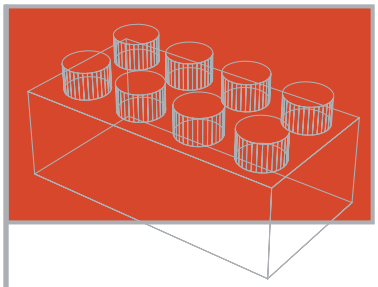
#	Operation	Module	Equipment	Physical	Chemical
510A	Implant Mask Photoresist Dispense	Photo	Coater / Developer	Dispense quantity, spin speed, spin time.	Photoresist (a light-sensitive material)

Purpose: This is the first stage the wafer goes through to create the source and drain of the transistor. Photoresist material will be exposed to UV light through the source/drain mask to define their boundaries.

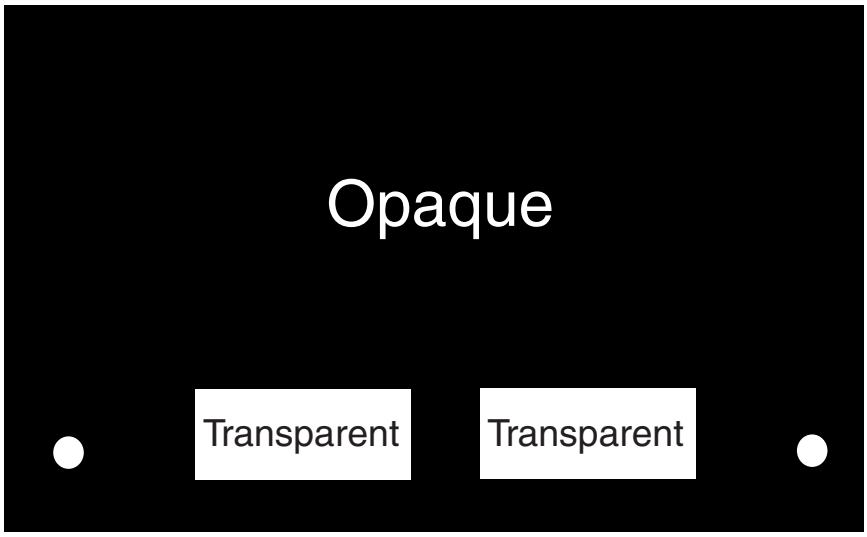
Procedure: Place the green photoresist blocks over the surface of the transistor. Follow the pattern indicated on the Photoresist Dispense template, as this will make it easier to perform the following operations on your substrate.

[Remember to fill out the Run Card]

N+ Source/Drain Implant Mask (Align & Expose)



Photo



Objective: The source/drain mask is aligned on top of the wafer. The heavily doped n-type material (n+) source/drain implant mask is used to create the locations of the source and drain on the transistor.

#	Operation	Module	Equipment	Physical	Chemical
510B	Align Mask	Photo	Stepper: Aligns substrate to the mask pattern.	Alignment accuracy is critical.	N/A
510C	Expose	Photo	Stepper: Uses UV light to expose photoresist.	The wafer is exposed to UV light. Energy and time of exposure are main parameters.	Photoresist (a light-sensitive material) that becomes acidic when exposed to UV light

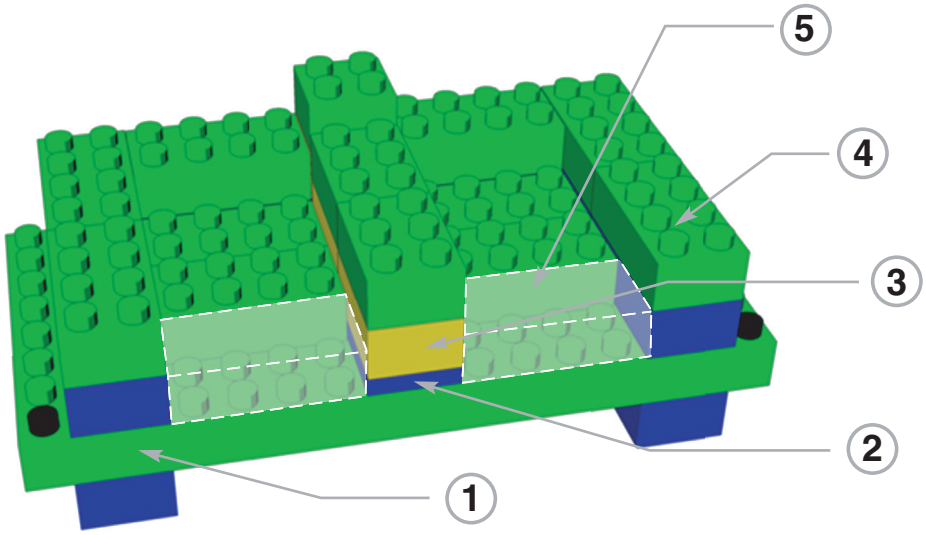
Purpose: In this step, the source/drain mask is aligned over the wafer, so that when the die is exposed to UV light through the source/drain mask, those areas of photoresist that received UV light (under the transparent rectangles), will be removed in the develop operation.

Procedure: Place the n+ source/drain implant mask over the transistor using the alignment marks. Shine the flashlight through the mask and notice the green photoresist blocks that are exposed to light.

[Remember to fill out the Run Card]

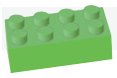
Implant Resist (Develop & Inspect)

Photo



1	Substrate
2	Gate Oxide
3	Polysilicon
4	Photoresist
5	Removed Photoresist

SUBTRACT



Objective: Remove the blocks of photoresist that were exposed to UV light. Then inspect the photoresist that was removed to make sure that the implant's locations are where they should be.

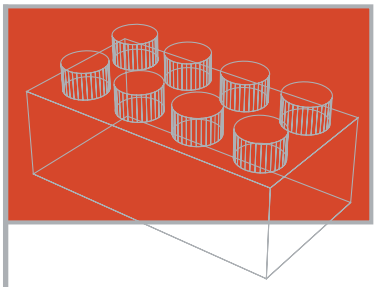
#	Operation	Module	Equipment	Physical	Chemical
510D	Implant Photoresist Develop	Photo	Coater / Developer	Dispense quantity, time, temperature, rinse, and spin speed	Exposed photoresist becomes acidic and is removed with a develop chemical by neutralizing its acidity.
515	Develop Inspect	Photo	Optical Microscope	Inspect the site of removed photoresist.	N/A

Purpose: The exposed photoresist removed in this develop process determines the actual locations for the source and drain of the transistor.

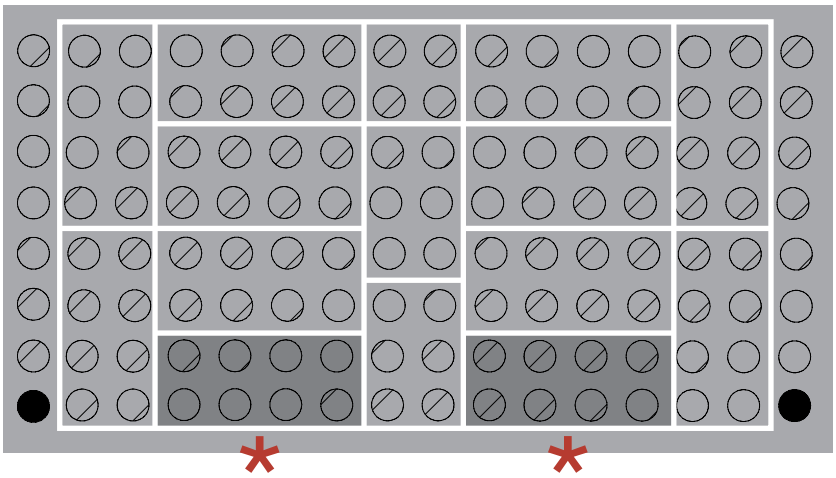
Procedure: From the previous step, remove only those blocks of photoresist (green blocks) that were exposed to light from the flashlight. Return these green blocks to the Photo module.

[Remember to fill out the Run Card]

Dopant Implant Template



Implant



* Place these dopant blocks underneath the substrate

Objective: Place dopant implants above and below the substrate as shown on the Dopant Implant Template.

#	Operation	Module	Equipment	Physical	Chemical
520	n+ Source / Drain Implant	Implant	Ion Implanter	Ions are accelerated through a high electrical charge to bombard the surface of the die.	Charged gaseous ions are used.

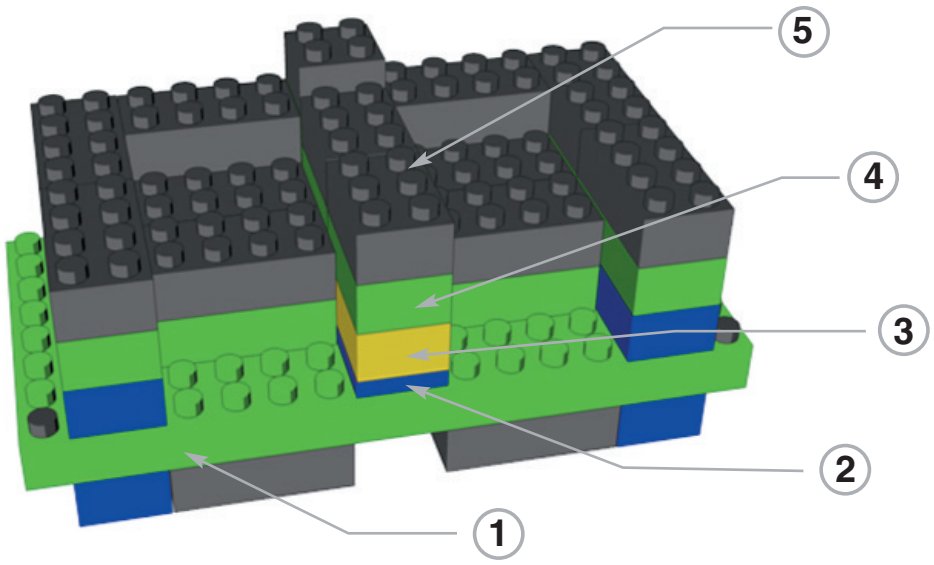
Purpose: Ions accelerated at very high voltage bombard the wafer at this point. These charged particles penetrate through exposed surfaces a very short distance, around 1 micron, which is why the black building blocks toward the front are actually underneath the green substrate. They are able to penetrate through the substrate because of the "windows" where photoresist was removed. The black layer (dopant implants) on the top should actually be embedded into the photoresist, but to keep this simulation simple and since this layer is going to be stripped away, their temporary presence makes no difference to the transistor's fabrication as a whole. The ions implanted into the surface of the source and drain locations change the electrical conductivity from a nonconductive to a semiconductive state. This will later allow electrons to flow from the source to the drain through a channel under the gate, when the gate is activated by the proper charge.

Procedure: Place the black blocks (dopant implant blocks) on the top of every exposed surface, following the dopant implant template. Also, place black blocks just underneath the surface of the source and drain locations.

[Remember to fill out the Run Card]

Source-Drain Implant

Implant



1	Substrate
2	Gate Oxide
3	Polysilicon
4	Photoresist
5	Dopant

ADD


12 2x4


2 2x3


1 2x2

This slide illustrates what the source/drain implant layer will look like when bombarding the substrate with ions has been completed.

Question #10

What is the purpose of the source and drain?

A. The source and drain allows for the removal of gate oxide by the use of a blend of acidic and basic chemicals.
B. The source and drain refers to the process of the local oxidation of the exposed silicon substrate.
C. The source and drain acts like a capacitor in that a charge can be stored in the dielectric.
D. The source and drain allows electrons to flow between them through a channel under the gate, when the gate is activated by the proper charge.

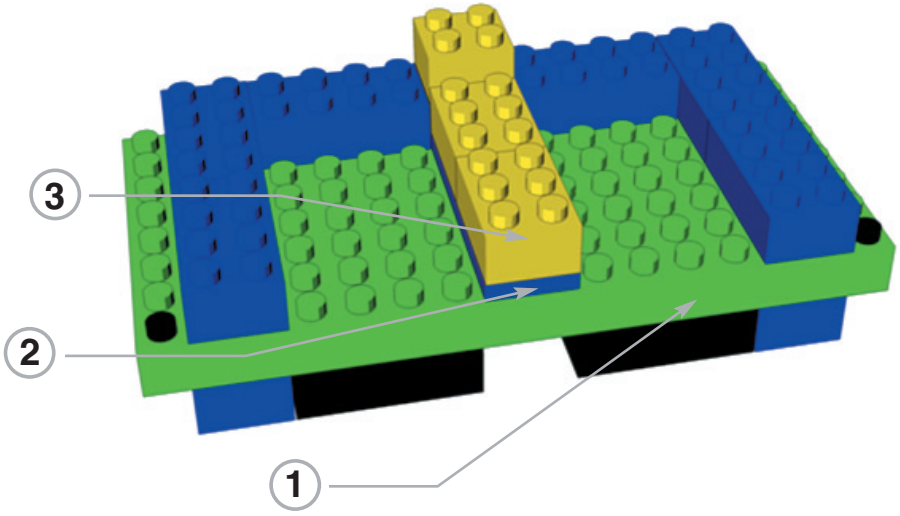
Answer: D

[Remember to fill out the Run Card]

Source-Drain Plasma Strip

1	Substrate
2	Gate Oxide
3	Polysilicon

Implant



Objective: All remaining photoresist is removed at this stage.

#	Operation	Module	Equipment	Physical	Chemical
525	N+ Source / Drain Plasma Strip	Implant	Plasma Resist Stripper	RF Power, chamber pressure, gas flow, temperature, time	Ionized oxygen is used to remove the photoresist.

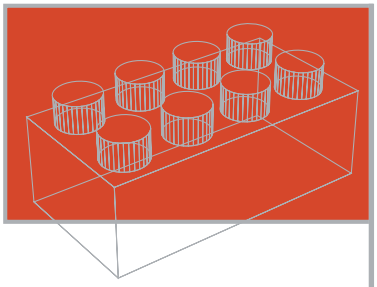
Purpose: In this stage, all remaining implanted photoresist is removed by oxygen ions in a plasma chamber.

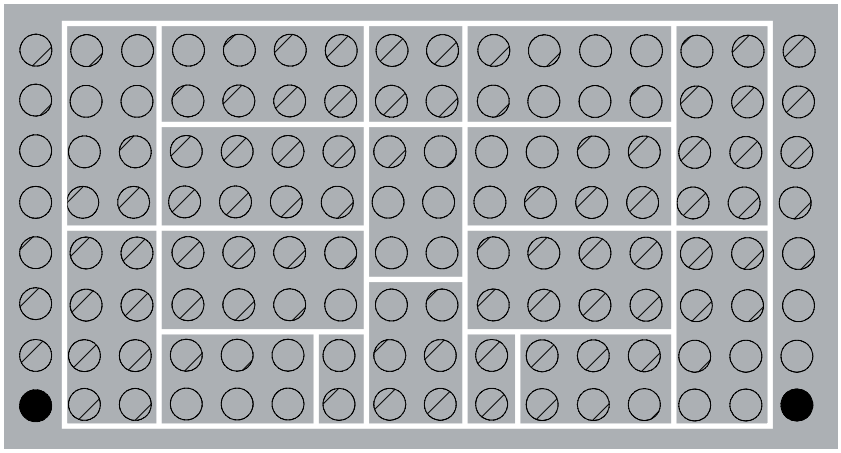
Procedure: Remove the top two surfaces of all black (dopant ions) and green (photoresist). Return the black blocks to the Thin Films module and the green blocks to the Photo module.

[Remember to fill out the Run Card]

Top Nitride Template

Thin Films





Objective: These last 16 steps (#'s 600 – 725 on the Run Card) will define the contacts of the source, drain, and gate of the transistor as well as provide protective material to cover the transistor itself. Begin by depositing a top layer of nitride onto the wafer as shown on the top nitride template.

#	Operation	Module	Equipment	Physical	Chemical
600	Top Nitride Mask Deposition	Thin Films	Low Pressure Chemical Vapor Deposition Furnace (LPCVD)	High temperature (~750°C), low pressure (~200 mtorr), gas flow rate, time	Dichlorosilane + Ammonia → $3SiCl_2H_2$ $4NH_3$ – Silicon Nitride + Byproducts Si_3N_4 $(6HCl + 6H_2)$

Purpose: Silicon nitride is deposited over the top of the wafer to serve as a protective layer. The top nitride is a thick film that protects the transistor from the environment.

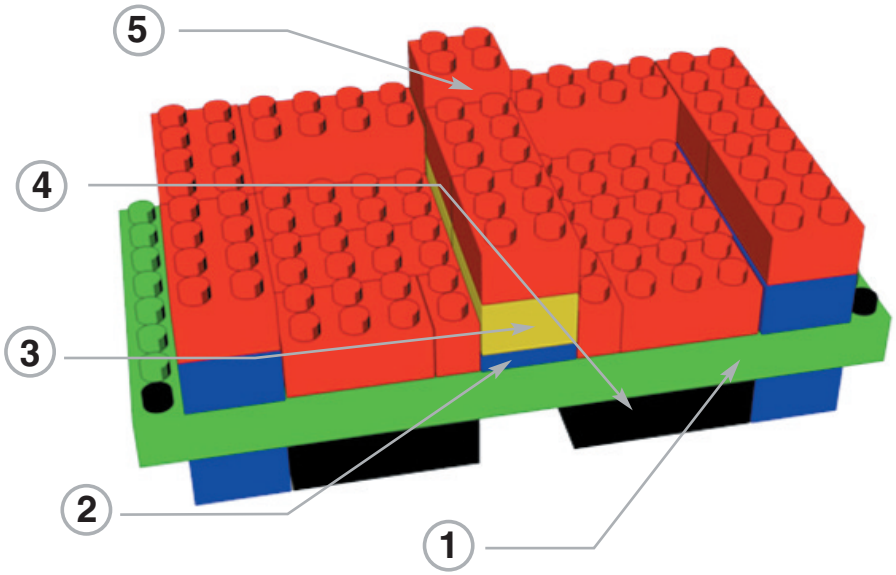
Procedure: Place the red (top nitride) blocks (using the top nitride mask template) over the surface of the transistor.

[Remember to fill out the Run Card]

Top Nitride Deposition

1	Substrate
2	Gate Oxide
3	Polysilicon
4	Dopant
5	Top Nitride
ADD	10 2x4
	4 2x3
	1 2x2
	2 2x1

Thin Films



This slide illustrates what the model should look like after a protective covering of top nitride is deposited over the surface of the wafer.

Question #11

What is the purpose of the top nitride layer?

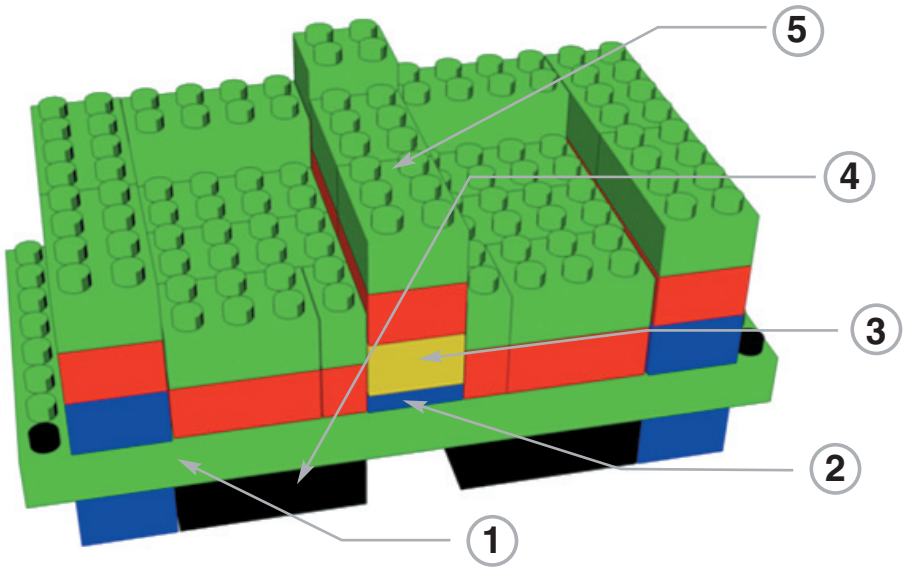
A. The top nitride layer acts as an insulating material that protects the transistor from the environment.
B. The top nitride layer is a positively charged material because it has a deficiency of electrons.
C. The top nitride layer, when exposed to light, becomes grainy and soluble and can be removed by a solvent.
D. The top nitride layer is a semiconductive material that forms the foundation of the transistor.

Answer: A

[Remember to fill out the Run Card]

Contact Mask Resist Dispense

Photo



1	Substrate
2	Gate Oxide
3	Polysilicon
4	Dopant
5	Photoresist
ADD	10 2x4
	4 2x3
	1 2x2
	2 2x1

Objective: Deposit photoresist on the substrate to match the pattern shown on the photoresist template.

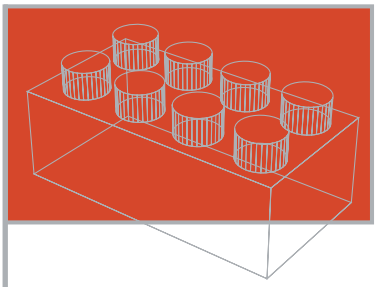
#	Operation	Module	Equipment	Physical	Chemical
610A	Contact Mask Photoresist Dispense	Photo	Coater / Developer	Dispense quantity, spin speed, spin time	Photoresist (a light-sensitive material)

Purpose: This represents the first step in photolithography. Photoresist is dispensed uniformly over the surface of the wafer.

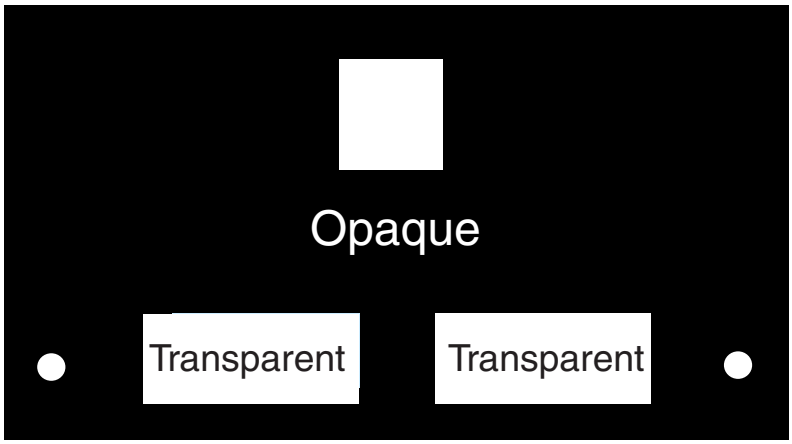
Procedure: Place the green photoresist blocks over the surface of the transistor. Follow the pattern indicated on the photoresist dispense template, as this will make it easier to perform the following operations on your wafer.

[Remember to fill out the Run Card]

Contact Mask (Align & Expose)



Photo



Objective: The contact mask (used to define the location of the source, drain, and gate contacts) is aligned on top of the substrate using the alignment marks. Light is used to expose the photoresist through the windows in the mask.

#	Operation	Module	Equipment	Physical	Chemical
610B	Align Contact Mask	Photo	Stepper: Aligns substrate to the mask pattern.	Alignment accuracy is critical.	N/A
610C	Expose	Photo	Stepper: Uses UV light to expose photoresist.	The wafer is exposed to UV light. Energy and time of exposure are main parameters.	Photoresist (a light-sensitive material) that becomes acidic when exposed to UV light

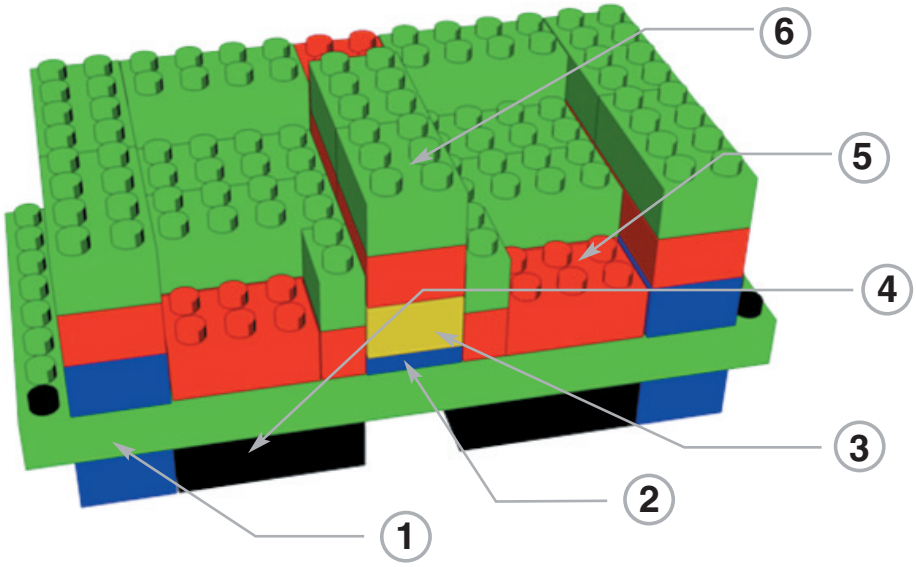
Purpose: In photolithography, after photoresist has been applied to the wafer's surface, the contact mask is placed over the transistor to get it ready for exposure to UV light. This mask alignment is a critical step as the size of the contacts is small, revealing where metal will have to be placed in order to make electrical contact.

Procedure: Place the contact mask over the transistor using the alignment marks. Shine the flashlight through the mask and notice the green photoresist blocks that are exposed to light.

[Remember to fill out the Run Card]

Contact Mask Resist Dispense

Photo



1	Substrate
2	Gate Oxide
3	Polysilicon
4	Dopant
5	Silicon Nitride
6	Photoresist
SUBTRACT	2 2x3
	1 2x2

Objective: Remove all photoresist that was exposed to UV light. These voids will serve as the location for the source, drain, and gate contact points. Then, inspect the photoresist that was removed to make sure that the contact's locations are where they should be.

#	Operation	Module	Equipment	Physical	Chemical
610D	Contact Mask Resist Develop	Photo	Coater / Developer	Dispense quantity, time, temperature, rinse, and spin speed	Exposed photoresist becomes acidic and is removed with a develop chemical by neutralizing its acidity.
615	Develop Inspect	Photo	Optical Microscope	Inspect the site of removed photoresist.	N/A

Purpose: In the develop operation, the exposed photoresist that is removed begins to define the three access points for electrical connections (contacts) of the transistor. In Defect Inspection (DI), make sure that the resist removed is supposed to be removed. Again, these are critical inspections since the size of the source, drain, and gate contact points are very small.

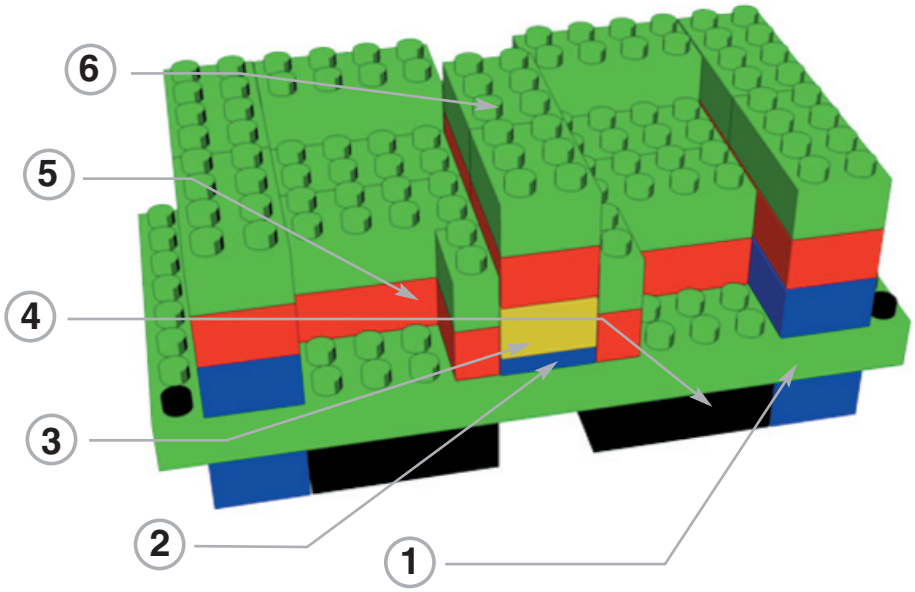
Procedure: Remove exposed photoresist (green blocks) from the model. Return the green blocks to the Photo module.

[Remember to fill out the Run Card]

Contact Etch

1	Substrate
2	Gate Oxide
3	Polysilicon
4	Dopant
5	Silicon Nitride
6	Photoresist
SUBTRACT	2 2x3
	1 2x2

Etch



Objective: All nitride that is not protected by photoresist is stripped away.

#	Operation	Module	Equipment	Physical	Chemical
620	Contact Etch	Etch	Dry Plasma Etcher	High-powered radio-frequency energy ionizing a gas inside a vacuum makes it easy to remove unwanted silicon nitride.	Flourine- or chlorine-based gases become highly reactive when ionized.

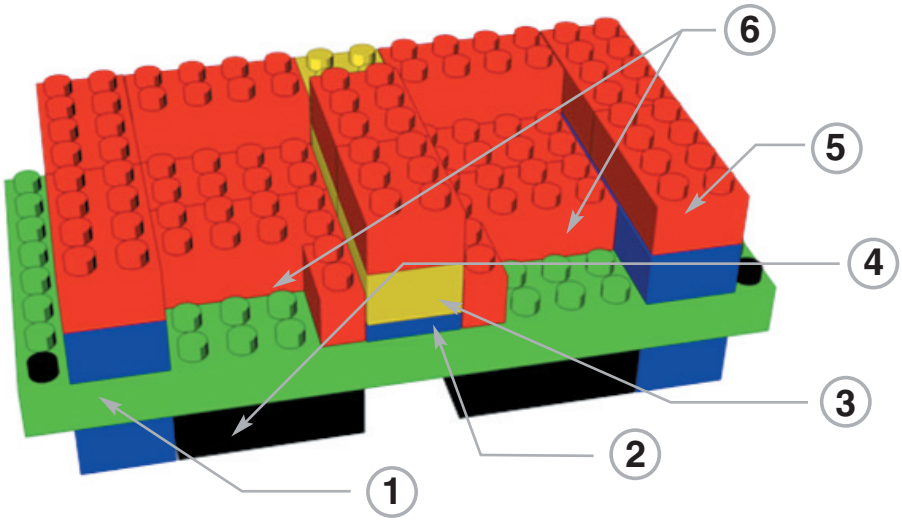
Purpose: Etching removes the nitride layer that is not protected by photoresist, basically the section of nitride over the three contact points. This etching process creates windows, providing access directly to the substrate level where the contact's locations will be defined.

Procedure: Remove the red blocks (silicon nitride) that are not covered by photoresist. Return the red blocks to the Thin Films module.

[Remember to fill out the Run Card]

Contact Resist Strip

Etch



1	Substrate
2	Gate Oxide
3	Polysilicon
4	Dopant
5	Silicon Nitride
6	Contact Holes

Objective: All remaining photoresist is removed in this operation.

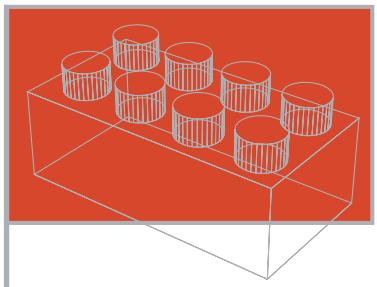
#	Operation	Module	Equipment	Physical	Chemical
625	Contact Resist Strip	Etch	Dry Plasma Etcher	RF Power, chamber pressure, gas flow, temperature, time	Ionized oxygen is used to remove the photoresist.

Purpose: It is at this stage that all photoresist that was remaining is removed. Notice that it took 9 steps to fully open up these contact windows directly into the substrate layer of the transistor.

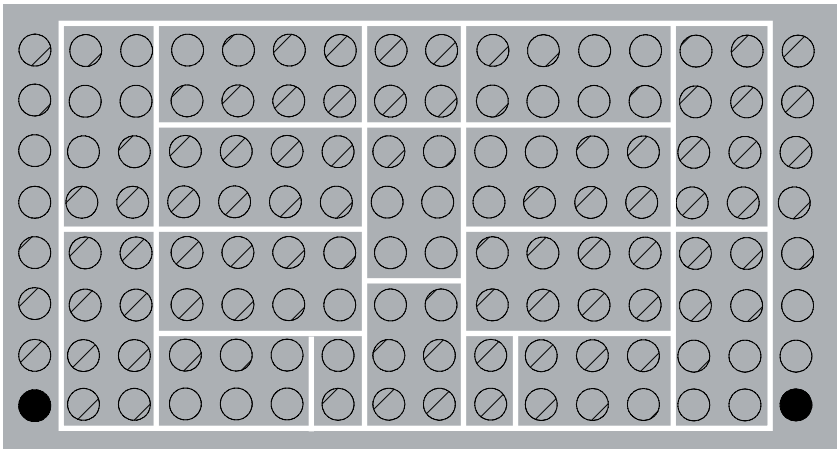
Procedure: Remove all remaining photoresist (green blocks) from the top surface of the wafer. Return all green blocks to the Photo module.

[Remember to fill out the Run Card]

Metal Template



Thin Films



Objective: A thin layer of metal is deposited over the entire surface of the wafer.

#	Operation	Module	Equipment	Physical	Chemical
700	Metal Deposition	Thin Films	Sputter, Physical Vapor Deposition (PVD)	Low pressure, temperature, metal, target, electromagnetic energy to ionize argon	Argon ions, aluminum, or a combination of titanium and tungsten.

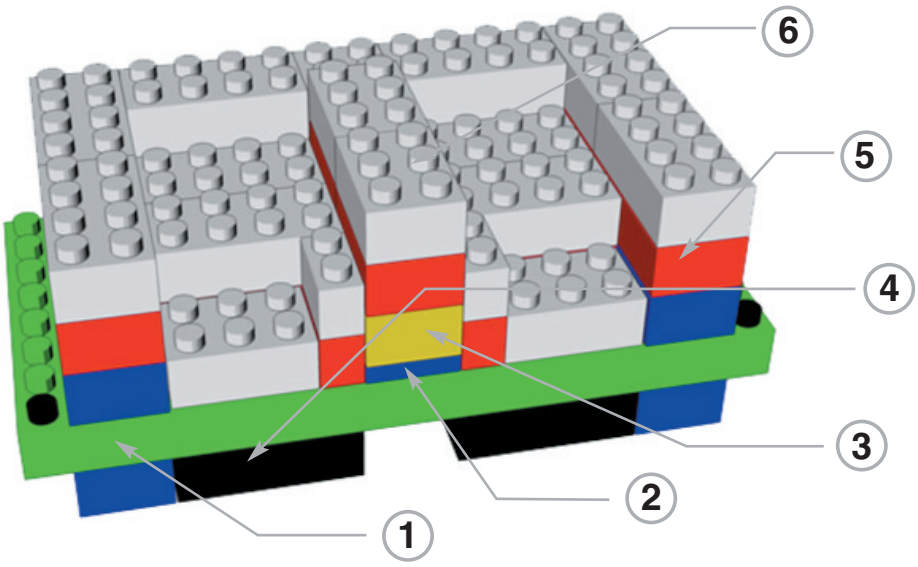
Purpose: Metal is deposited over all exposed areas on the top surface of the model. Metal will serve as conductive material for the source, drain, and gate contacts. Sputtering, or the physical vapor deposition (PVD), is the act of bombarding a targeted metal, such as aluminum, with argon ions and breaking up the metal molecules of the target so that they settle down over the surface of the wafer.

Procedure: Place the metal layer (white blocks) over the surface of the transistor following the metal template.

[Remember to fill out the Run Card]

Metal Deposition

Thin Films



1	Substrate
2	Gate Oxide
3	Polysilicon
4	Dopant
5	Silicon Nitride
6	Metal Layer

ADD


10 2x4


4 2x3


1 2x2


2 2x1

This slide illustrates what the wafer should look like after the layer of white blocks, representing the thin metal layer, has been distributed over the top surface of the wafer.

Question #12

What is the purpose of the metal layer?

A. The metal layer serves as conductive material to connect the electrodes together.
B. The metal layer is the material of which the gate structure is made.
C. The metal layer serves as the material from which the electrodes that will allow electrical connections of the transistor will be formed.
D. The metal layer provides the thick, protectant film for the transistor.

Answer C

[Remember to fill out the Run Card]

Metal Mask Resist Dispense

1	Substrate
2	Gate Oxide
3	Polysilicon
4	Dopant
5	Silicon Nitride
6	Photoresist

ADD

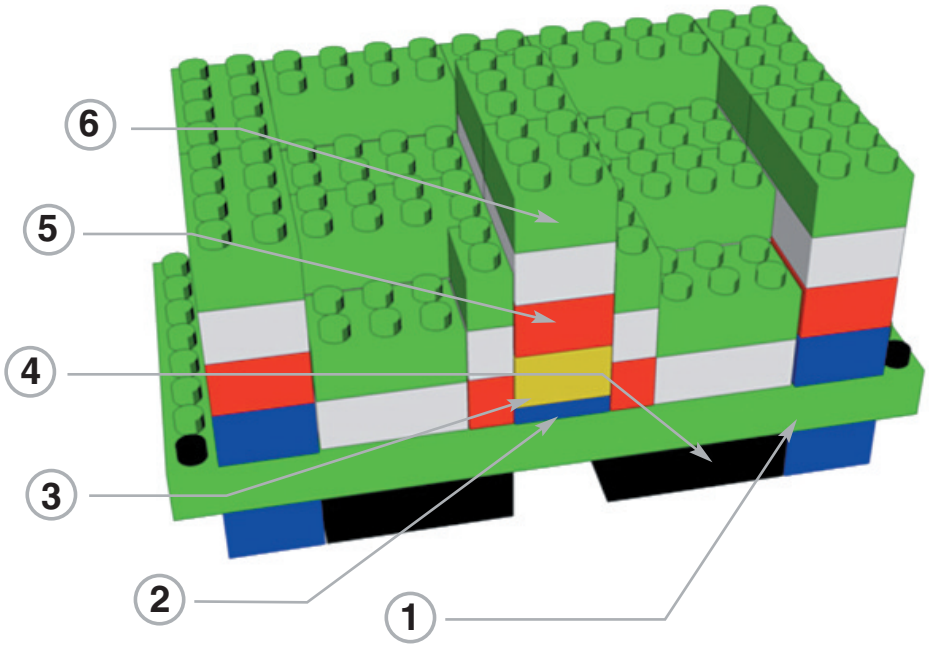

10 2x4


2 2x3


2 2x2


2 2x1

Photo



Objective: Deposit photoresist on the substrate to match the pattern shown on the photoresist dispense template.

#	Operation	Module	Equipment	Physical	Chemical
710A	Metal Mask Photoresist Dispense	Photo	Coater / Developer	Dispense quantity, spin speed, spin time	Photoresist (a light-sensitive material)

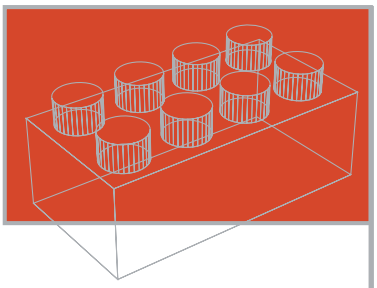
Purpose: This is the second time that the wafer begins the 4-step photo process toward defining the three contact points. Again, the objective of this series of steps is to define the source, drain, and gate contact points.

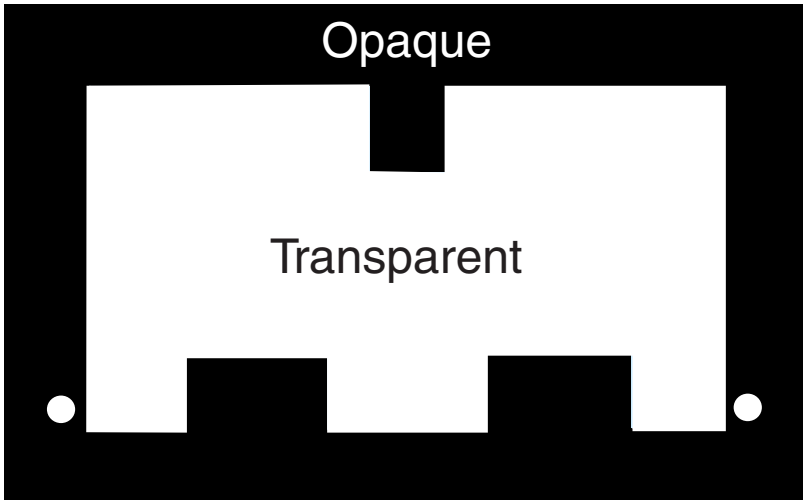
Procedure: Place the green photoresist blocks over the surface of the transistor. Follow the pattern indicated on the photoresist dispense template, as this will make it easier to perform the following operations on your wafer.

[Remember to fill out the Run Card]

Metal Etch Mask (Align & Expose)

Photo





Objective: In this step, align the metal etch mask over the wafer and expose the photoresist through the mask.

#	Operation	Module	Equipment	Physical	Chemical
710B	Align Metal Etch Mask	Photo	Stepper: Aligns substrate to the mask pattern.	Alignment accuracy is critical.	N/A
710C	Expose	Photo	Stepper: Uses UV light to expose photoresist.	The wafer is exposed to UV light. Energy and time of exposure are main parameters.	Photoresist (a light-sensitive material) that becomes acidic when exposed to UV light

Purpose: By the time that this metal etch mask will be aligned over the wafer, photoresist will have already been deposited on the surface of the wafer. The transistor, with the metal etch mask in place, will be ready to be exposed to UV light.

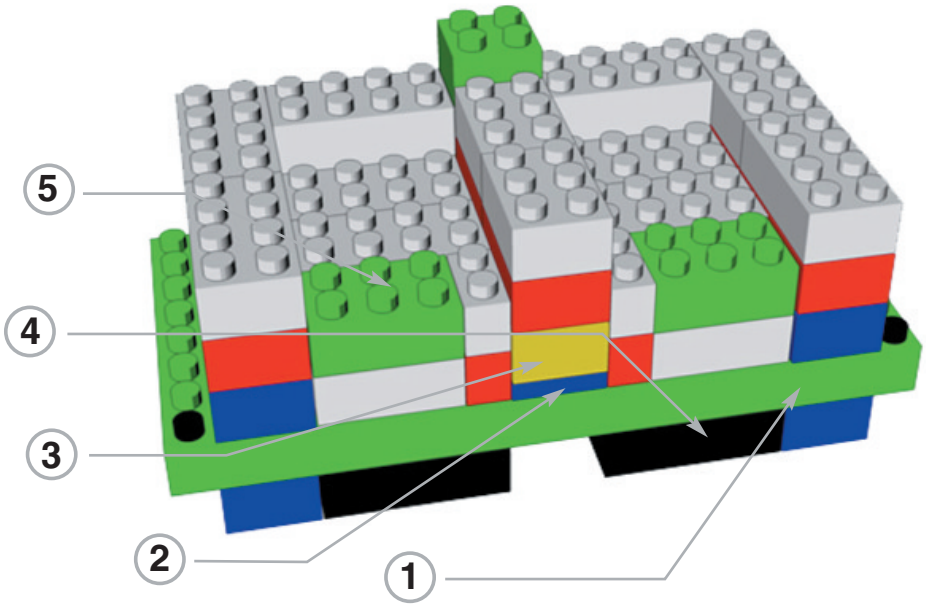
Procedure: Place the metal etch mask over the transistor using the alignment marks. Shine the flashlight through the mask and notice the green photoresist blocks that are exposed to light.

[Remember to fill out the Run Card]

Metal Etch Mask Resist (Develop & Inspect)

1	Substrate
2	Gate Oxide
3	Polysilicon
4	Dopant
5	Photoresist
SUBTRACT	10 2x4
	2 2x3
	2 2x1

Photo



Objective: Photoresist that has been exposed to UV light will be removed with the develop process.

#	Operation	Module	Equipment	Physical	Chemical
710D	Metal Etch Mask Resist Develop	Photo	Coater / Developer	Dispense quantity, time, temperature, rinse, and spin speed.	Exposed photoresist becomes acidic and is removed with a develop chemical by neutralizing its acidity.
715	Develop Inspect	Photo	Optical Microscope	Inspect the site of removed photoresist.	N/A

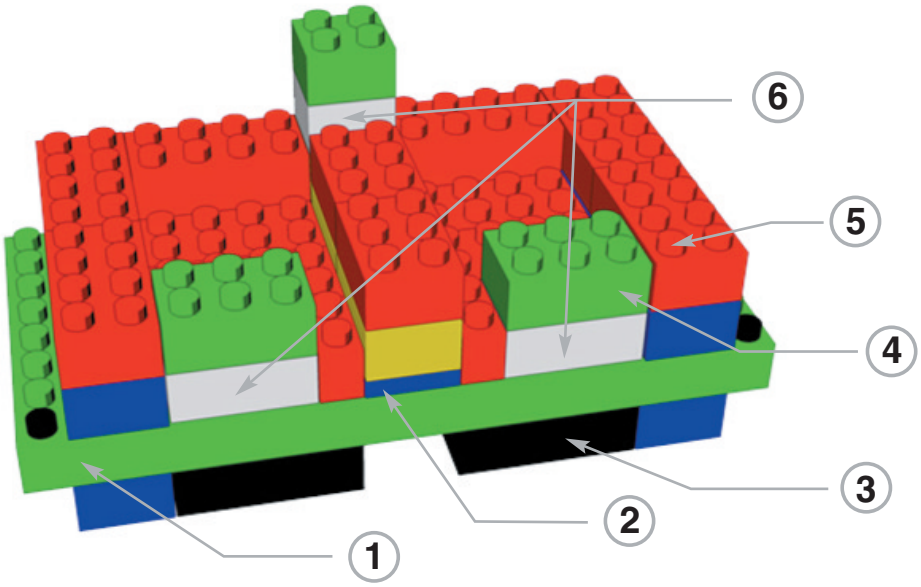
Purpose: Exposed photoresist will be removed in this step. Basically, all photoresist will be removed except for the photoresist covering the three metal contacts.

Procedure: Remove exposed photoresist (green blocks) from the surface of the wafer. Return the green blocks to the Photo module.

[Remember to fill out the Run Card]

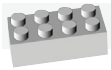
Metal Etch

Etch



1	Substrate
2	Gate Oxide
3	Dopant
4	Photoresist
5	Top Nitride
6	Metal Contacts

SUBTRACT

 10 2x4

 2 2x3

 2 2x1

Objective: All metal not protected by photoresist is removed from the wafer.

#	Operation	Module	Equipment	Physical	Chemical
720	Metal Etch	Etch	Dry Plasma Etcher	High-powered radio-frequency energy ionizing a gas inside a vacuum makes it easy to remove unwanted polysilicon.	Flourine- or chlorine-based gases become highly reactive when ionized.

Purpose: Metal that is not covered by photoresist is removed in this step. This strips all metal away (except that covered by photoresist on top of the three contact points) so that there will be no short-circuiting of the source, drain, and gate of the transistor.

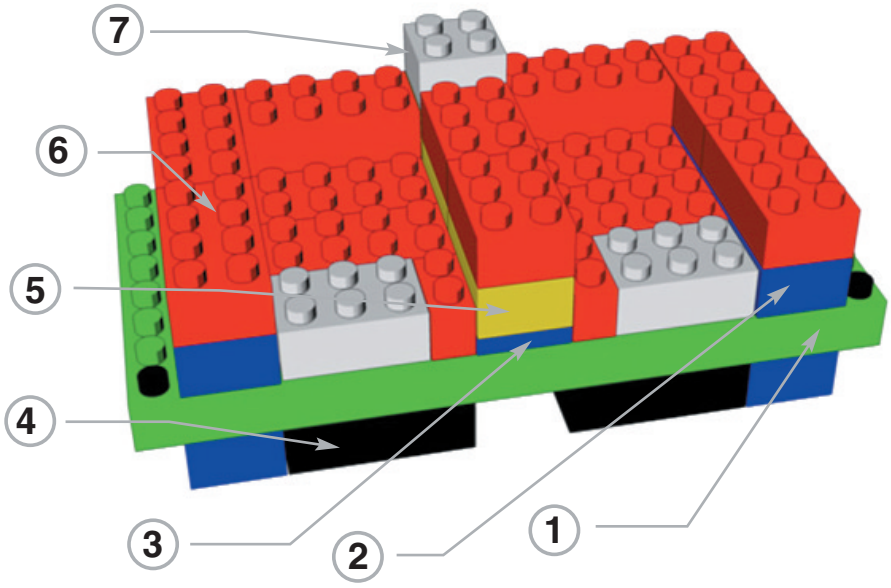
Procedure: Remove the white blocks (metal layer) that are not covered by photoresist. Return the white blocks to the Thin Films module.

[Remember to fill out the Run Card]

Metal Resist Strip

1	Substrate
2	Silicon Nitride
3	Gate Oxide
4	Source & Drains
5	Polysilicon Gate
6	Top Nitride
7	Metal Contacts

Etch



Objective: Remove all remaining photoresist.

#	Operation	Module	Equipment	Physical	Chemical
725	Metal Resist Strip	Etch	Solvent Station	Temperature, time	Solvent is used to remove photoresist rather than acid or base chemicals.

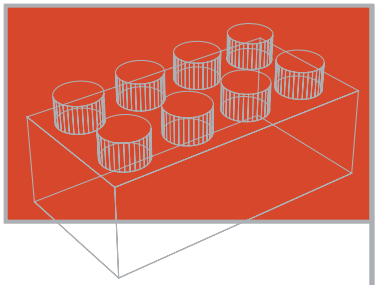
Purpose: In this step, the remaining traces of photoresist are removed. Basically, the only photoresist that was left over covered the three contact points. The contact points are now exposed and are ready to be used as connectors with other elements on this die. This is basically the last step towards making one MOS transistor, and the end of this simulation.

Procedure: Remove all remaining photoresist (green blocks) from the top surface of the wafer. Return the green blocks to the Photo module.

[Remember to fill out the Run Card]

The End

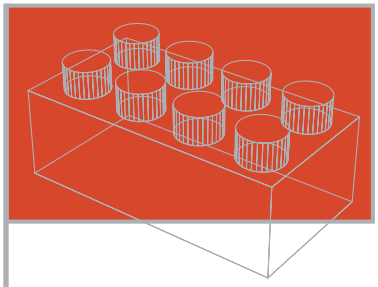
This concludes the Transistor Model Assembly Procedure.



Post-assembly Activities

1. Place two transistor models on a table facing each other. The combined pair actually form one transistor with field oxide completely surrounding the transistor.
2. Place additional models side by side to form a transistor pair as in a CMOS inverter circuit.
3. Brainstorm with your team members what steps would need to be taken in order to connect several transistors together using some of the materials, concepts, and procedures you learned in this activity.
4. Brainstorm with your team members the answers to the following questions:
   - **A.** Which modules are the busiest during the front end of the transistor fabrication process?
   - **B.** Which modules are the busiest during the back end of the transistor fabrication process?
   - **C.** Which are the busiest modules in the transistor fabrication process?
   - **D.** Which module in the transistor fabrication process controls the accuracy of the placement and sizes of the structures being formed?
   - **E.** Would you now say that transistors are two- or three-dimensional structures?
   - **F.** Which is the thinnest film in the entire process?
   - **G.** In the actual transistor fabrication process, which is the only operation that can be reworked?
5. Share any thoughts you may have with your instructor and fellow classmates regarding this activity. What did you gain from it? Has it helped you gain a better understanding of the complex steps inmanufacturing semiconductor devices?

The Five Modules in a Wafer Fab



In this simulation, there are five basic process module departments that handle specific manufacturing processes of a transistor. Each module is a collection of similarly related processes that can be grouped together, such as photolithography. The five modules are listed below giving a brief description of the module's operation, the equipment used, and what the equipment does.

Photo: involves the process of printing an image onto the surface of the wafe.

Coater / Developer: spins the wafer at a given speed while it dispenses photoresist onto the wafer. It also develops the images transferred to the wafer during exposure to UV light.

Stepper: the camera that exposes the photoresist on the wafer to UV light, passing through a mask which contains the original image

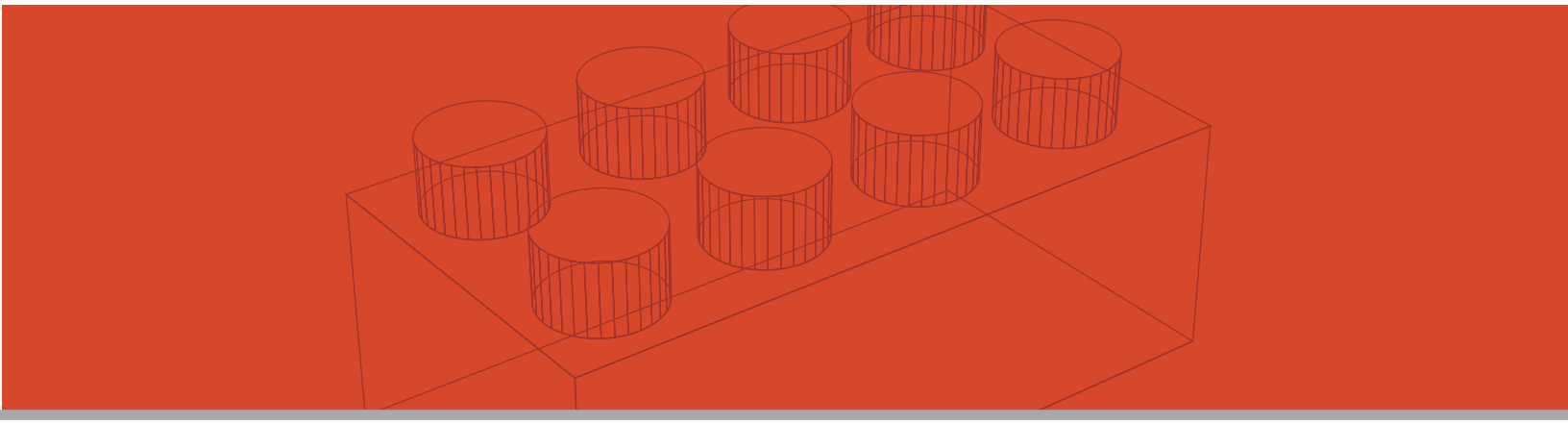
Etch: a 2-step process takes place here

1st: permanently inscribes the photo pattern onto the wafer by removing material not covered by photoresist

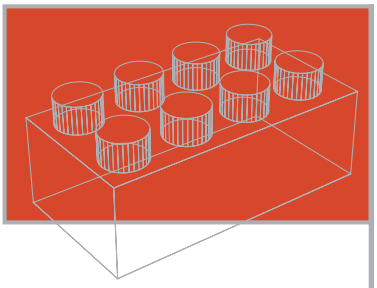
2nd: removes any remaining photoresist

Dry Plasma Etcher: chlorine- or fluorine-based gases, ionized by high RF energy, become highly reactive to remove any unwanted material. Used to remove nitride, polysilicon, and metals.

Plasma Stripper: removes all remaining photoresist after the etching is done



Diffusion: used for depositing materials onto the wafer's surface, with furnaces as hot as 1200° C (close to the temperature at which silicon starts to melt and forms glass)



Low Pressure Chemical Vapor Deposition (LPCVD): high-temperature, low-pressure furnace used to apply the initial nitride layer and polysilicon

High Temperature Furnace: used to grow field oxide

Thin Films: used for the application of thin films of material onto the wafer's surfac. CVD tools are used here instead of furnaces as in diffusion

Chemical Vapor Deposition (CVD): used to deposit the top nitride layer

Physical Vapor Deposition (PVD): also referred to as sputtering, uses radio-frequency (RF) power to charge up argon ions to bombard a targeted metal, such as aluminum, to dislodge particles of the metal so that they settle down and form a metal layer on the wafer

Ion Implant: a high-energy process that injects an ionized species such as boron or arsenic into a substrate using an ion beam, to change the material bombarded from semiconductive to conductive

Ion Implanter: adds dopants to the wafer, using high voltages, through a partially patterned, resist-coated wafer

Plasma Stripper: removes all remaining photoresist after the implanting is done

Glossary

angstrom (Å): A unit of measure equal to one ten billionths of a meter, or 1 x 10^{-10} m. The diameter of a human hair is approximately 750,000 Å. Because of its size, angstroms are used to describe atomic and small semiconductor device dimensions, such as gate structures.

capacitor: Electronic component made up of two conductive plates separated by a dielectric. It can be used to store an electric charge.

CVD: Chemical Vapor Deposition. A process in which a controlled chemical reaction produces a thin surface film.

channel: A thin region between the source and drain of the MOS transistor which is itself the conduit for electron flow when the transistor's gate is activated by the proper charge.

conductor: A substance through which electricity can readily flow, as opposed to an insulator. Metals are good conductors of electricity.

deposition: An operation in which a film is placed on a wafer without a chemical reaction with the underlying layer.

die: A small piece of silicon wafer, enclosed by boundary horizontal and vertical boundary lines, that contains the complete device being manufactured. Also referred to as a chip or microchip.

dielectric: A nonconductive material, or insulator. Examples are silicon dioxide and silicon nitride. One use of a dielectric is to serve as the insulating material found between the plates of a capacitor that is able to store electric charge.

diffusion: A high-temperature process in which desired chemicals (dopants) on a wafer are redistributed within the silicon to form a device component.

dopant: A chemical element incorporated in trace amounts in a semiconductor layer to establish its conductivity type and resistivity. For example, dopants are added to silicon to produce p-type or n-type semiconductor material.

drain: One of the three electrodes of a MOS transistor where charge carriers leave the channel.

FOx: Field Oxide *(see oxide)*

etch: A process of removing material from selected areas of a die. Examples are nitride etch and oxide etch. This process uses a mixture of solutions or gases that attacks the surface of a film or substrate removing material selectively.

gate: One of the three electrodes of a MOS transistor that regulates the flow of current between the source and the drain. It is also referred to as the input of the transistor.

glass: A deposited film of silicon dioxide (SiO_2) on a wafer because of its insulating characteristics. Also referred to as oxide.

Glossary

GOx: Gate Oxide *(see oxide)*

holes: Positively charged carriers found in silicon crystal that has been doped with p-type dopant, e.g., boron.

IC: Integrated Circuit. Two or more interconnected circuit elements on a single die. A fabrication technology that combines most of the components of a circuit on a single-crystal silicon wafer.

insulator: A substance(e.g., silicon dioxide and silicon dioxide) that will not conduct electricity, as opposed to a conductor. Insulators are used in capacitors as dielectrics.

ion: An atom that has gained or lost electrons making it a charged particle.

ion implantation: A high-energy process that injects an ionized species such as boron, phosphorous, or arsenic into a semiconductor substrate, using an ion beam.

LPCVD: Low Pressure Chemical Vapor Deposition, similar to CVD

MOS: Metal Oxide Semiconductor. The type of transistor built in the transistor model assembly kit.

mask: A flat, transparent plate that contains the photographic image of wafer patterns necessary to define one process layer of a transistor.

metallization: The deposition of a thin film of conductive metal onto a wafer or substrate by use of physical vapor deposition (e.g., sputtering).

micron: A metric unit of linear measure (m) that equals 1/1,000,000 meter (1×10^{-6} m), or 10,000 angstroms. The diameter of a human hair is approximately 75 microns.

n+: Heavily doped regions in the silicon implanted with n-type dopant.

n-type material: Describes a semiconductor material that has negatively charged conductivity (a surplus of electrons), formed when donor impurities are incorporated into the crystal structure in small concentrations.

nitride: Silicon nitride (Si_3N_4) is a layer that is chemically deposited on a wafer to protect the wafer from contamination. It is used as a masking layer and as an insulator.

nitride etch: An etch process whereby unprotected portions of a silicon nitride layer are eroded to expose the initial oxide layer beneath the nitride.

oxidation: A high-temperature chemical reaction in which the silicon of the wafer surface reacts with oxygen to form an oxide such as silicon dioxide.

oxide: A dielectric or nonconducting film grown or deposited on the surface of a wafer. Oxide refers to silicon dioxide, the insulator or dielectric most commonly used in MOS devices. Examples are field oxide (which insulates the transistor's operations from other nearby transistors), and gate oxide (which serves as the dielectric insulator between the gate polysilicon and the silicon substrate).

Glossary

p-type material: A material that has positively charged conductivity (a deficiency of electrons). It also describes a variety of semiconductive material in which the majority current carriers are holes, formed when acceptor impurities are incorporated into the crystal structure in small concentrations.

photolithography: A process in which a masked pattern is projected onto a photosensitive coating that covers a substrate.

photoresist: A light-sensitive material that, when applied to a substrate and then exposed and developed, transfers patterns onto itself through the mask that was used.

PVD: Physical Vapor Deposition. A process whereby films of material, usually metals, are deposited by physical means— for example, sputtering.

plasma: Ionized gas used to remove resist, to etch, or to deposit various layers onto a wafer. Plasma is generated by strong radio-frequency (RF) fields. A side effect of plasma gas is that it glows, an example of which is the glow of plasma in neon lights.

plasma etch: Processes that use a mixture of physical and chemical etching that employ reactive ionized gas to remove unprotected portions of a layer of material.

radio frequency (RF): Electromagnetic energy with frequencies ranging from 3 kHz to 300 GHz. Microwaves are a portion of radio frequency extending from 300 MHz to 300 GHz.

semiconductor: An element that has an electrical resistivity in the range between conductors (such as aluminum) and insulators (such as silicon dioxide). Integrated circuits are typically fabricated in semiconductor materials such as silicon, germanium, or gallium arsenide.

source: One of the three electrodes of a MOS transistor that is in the output section of a transistor from which charge carriers enter the channel.

sputtering: An operation in which a target material, such as gold or aluminum, is bombarded with argon ions. The displaced molecules of the target material are then deposited on the wafer surface.

stripper: A chemical solvent used to remove resist film from wafers.

substrate: A wafer that is the basis for subsequent processing operations in the fabrication of semiconductor devices or circuits.

transistor: A semiconductor device whose three major components are a gate, source, and drain. Transistors are capable of amplifying an input voltage, or acting as a switch or logic gate.

wafer: A thin slice with parallel faces cut from a semiconductor crystal.

wet etch: A physical etch process that uses chemicals such as hydrofluoric acid to remove unprotected areas of a wafer layer.